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Technical Note TN-202 **Version 1.0**

Technical Product Information for the DAP 1200a™

The DAP 1200a models

- each have an on-board Intel 80C186XL 16-MHz or 20-MHz processor
- are completely compatible with other a-Series boards
- work with the PC/AT/ISA bus for 286/386/486 PC or Pentium platforms
- transfer data at high rates: up to 312K samples per second
- allow fast real-time processing
- offer low latency—1 ms per task—for fast response
- sample analog or digital inputs at rates up to 312K samples per second
- update analog outputs at rates up to 312K samples per second each
- update digital outputs at rates up to 312K samples per second
- each have expandable analog and digital inputs/outputs

This technical note describes all of the DAP 1200a models in terms of their similarities with other a-Series boards, software speed and functionality, and their hardware characteristics.

There are two DAP 1200a models: the DAP 1200a/4, and the DAP 1200a/6. Their hardware differs in two areas: speed of the on-board CPU and sampling rate. The DAP 1200a/4 has a 16-MHz 80C186XL and can sample at rates of up to 166K samples per second. The DAP 1200a/6 has a 20-MHz 80C186XL, and can sample at rates of up to 312 Ksamples per second.

The DAP 1200a models have the same aquisition and CPU processing power of the DAP 2400a-Series. However, they do not have the DSP 56001 co-processor. The DAP 1200a is appropriate for intelligent data aquisition and control applications where fast real-time digital signal processing is not required. The DAP 1200a can still emulate all the standard DAPL DSP routines on the 80C186XL, performing them at rates applicable for lower speed applications.

The DAP 1200a models are completely compatible with other a-Series boards and may be exchanged with them in any configuration. The cabling diagram at the end of this document gives a number of typical configurations. These configurations all use the same termination and expansion boards.

The onboard multi-tasking operating system, DAPL ™, is common to all a-Series boards and ensures that hardware-level differences are transparent. DAPL is a complete software environment for real-time data acquisition. To aid application development, DAPL comes complete with many system diagnostics, in addition to automatic memory and system checks that are done at initialization. Tasks that perform averaging, triggering, FFTs, filtering, arithmetic operations, or many other functions are pre-coded in DAPL. These tasks, or DAPL commands, are chained together to form a complete data aquisition application. Custom commands can also be written using the Developer's Toolkit for DAPL™ if multiple commands need to be combined or if a very specific application cannot be achieved with standard DAPL commands. Table 1 lists some standard DAPL commands with their speed of execution on the DAP 1200a.

Another common element shared by the a-Series boards is the bus interface. The DAP 1200a works with the PC/AT/ISA bus for 286/386/486/Pentium industry standard platforms. On a-Series Data Acquisition Processors, 1K bidirectional FIFO buffers allow fast data transfer to and from the host PC. The maximum transfer rates for the DAP 1200a are 312K samples per second to send data to the PC, and up to 519K samples per second to transfer information from the PC to the DAP 1200a.

The main feature of the DAP 1200a is its low-cost solution to data acquisition and real-time processing. The DAP 1200a is an excellent choice for applications where there is a need for real-time triggering, averaging, control, interpolation or a host of other functions, but no special high-speed requirements for FFTs or complex digital filtering. Table 1 gives information about the execution speed of DAPL commands on the DAP 1200a.

DAPL Command	Description	Time of Execution[1] on DAP 1200a/4	Time of Execution on DAP 1200a/6
`AVERAGE`	Averages groups of 16 data points[2]	88 µs	70.4 µs
`FFT`	FFT of blocksize of 512 points	151 ms	119 ms
`RFILTER`	Filters input data with 20 tap filter	198.75 µs	157.6 µs
`LIMIT`	Generates level based triggers on 1% of data	5.5 µs	4.8 µs
`WAIT`	Processes data based upon triggers at a retention rate of 5 out of 100 samples	3.75 µs	2.4 µs
DAPL Expression : `P3 = P1 + P2`	Adds two word-length pipe values together	40.0 µs	30.8 µs

Table 1: DAPL command execution speed for the DAP 1200a/4 and DAP 1200a/6

In addition to high performance processing, the DAP 1200a provides the standard arrangement of complete analog/digital input and output sections. These analog and digital sections are completely expandable — see Table 2 for complete specifications.

Data is sent or received by the DMA controller of the 80C186XL at a rate of up to 312K samples per second. This data is clocked at a sampling rate or output rate controlled in software, but the actual rate is accurately set by onboard crystal-controlled timers. The sample period is specified in steps as small as a fifth of a microsecond. The length of every sample period is accurate to 50 parts per million.

In addition to on-board timing, the DAP 1200a also has provisions for external triggering and clocking for the input and output sections.

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[1] The speed given is an actual application speed for the DAPL task, including sampling, DAPL task-switching and activation, and simulated transfer time. Kernel speeds for the tasks are actually faster.

[2] The speed given is also for the complete block operation, if applicable. For a per value speed, the time of execution must be divided by the block size.

Note that the digital and analog output sections of the DAP 1200a cannot be updated synchronously at the same time.

To clarify the operation for the various hardware sections, Figure 1 displays the architecture of the processing hardware of the DAP 1200a.

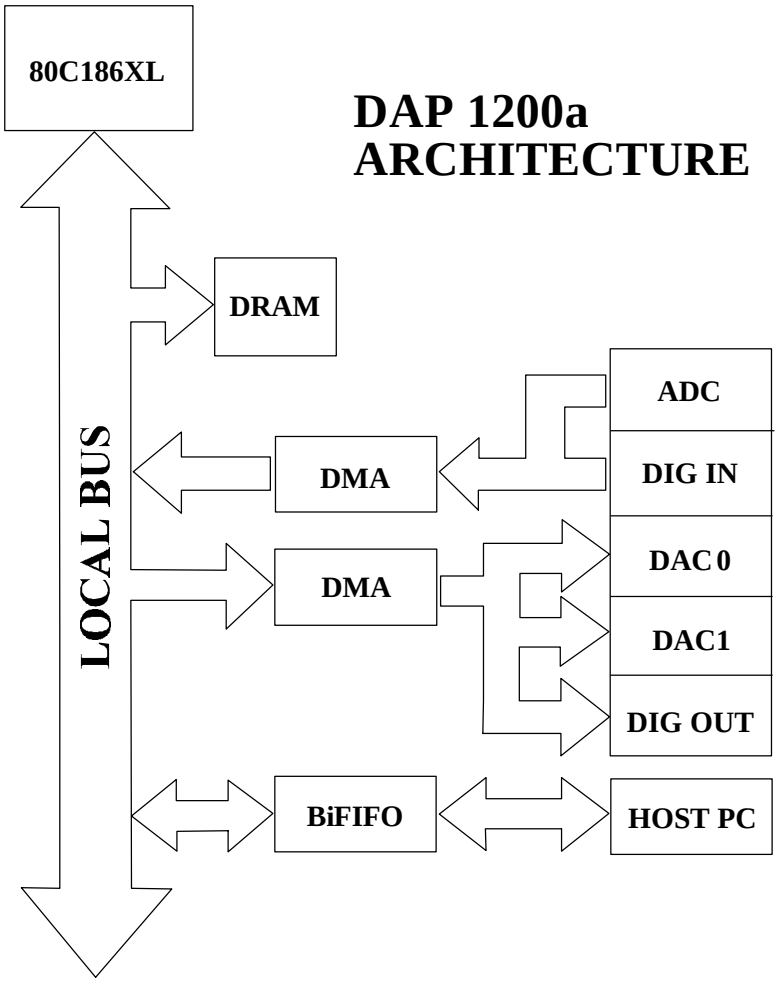

Figure 1: DAP 1200a Data Acquisition Hardware

In this figure, the 80C186XL processor shown performs the operations necessary for data acquisition and control. The CPU resides upon the local Data Acquisition Processor bus and transfers information between the input and output sections and the host PC. For instance, data from the analog and digital inputs are sent via DMA transfers to the processor DRAM. From there it can be processed by the CPU, transferred to the PC, and/or directed to the output section.

Transfer of data and other communication to the PC is handled by a BiFIFO. Information can be exchanged with the PC in both directions simultaneously, and can be either DAPL programs, binary or text data, error messages, or DAPL system commands. This communication method is not only

faster than DMA, but allows multiple Data Aquisition Processor boards to share one interrupt line. In this way, up to fourteen DAP 1200a boards can control and acquire data in one PC.

In addition to the processor and data transfer hardware, some important hardware specifications of the DAP 1200a are given below:

Table 2: DAP 1200a Typical Hardware Specifications

Specification	DAP 1200a/4	DAP 1200a/6
Dimensions	13.33" x 4.8"	13.33" x 4.8"
Weight	9.9 oz	9.9 oz
CPU Type	Intel 80C186XL	Intel 80C186XL
CPU Clock Speed	16 MHz	20 MHz
CPU DRAM	1 Mbyte	1 Mbyte
Data Acquisition Mode	DMA	DMA
Bus Support	AT	AT
PC Interface Hardware	1 Kbyte FIFO buffer	1 Kbyte FIFO buffer
PC Transfer Mode	I/O Interrupt	I/O Interrupt
Maximum Transfer Rate	166K samples/sec	312K samples/sec
Power Requirements	+5V, 2.3 Amps	+5V, 2.3 Amps
Operating Temperature	0-50 °C	0-50 °C
Accuracy of Crystal Clocks	50 parts per million	50 parts per million
Type of A⇒D Converter	Successive Approximation	Successive Approximation
Model of A⇒D Converter	Burr-Brown ADS7800	Burr-Brown ADS7800
Max. Analog Sampling at Gain = 1 Gain = 10 Gain = 100 Gain = 500	 166 K samples/sec 125 K samples/sec 25 K samples/sec 2 K samples/sec	 312 K samples/sec 125 K samples/sec 25 K samples/sec 2 K samples/sec
Number of Analog Input Channels	16	16
Expandable To	512	512
Input Voltage Ranges	0 to 5 V -5 to 5 V -10 to 10 V	0 to 5 V -5 to 5 V -10 to 10 V
Resolution If Range is -5 to 5 Volts	12 bits 2.4 mV	12 bits 2.4 mV
Accuracy If Range is -5 to 5 Volts	±1 LSB ±2.4 mV	±1 LSB ±2.4 mV
Bias Current	12 nA	12 nA
Analog Input Impedance	>> 10 MΩ	>> 10 MΩ
Common Mode Rejection	90 dB	90 dB
Max. Input Voltage (Fault-protected)	±25 V	±25 V

Table 2: DAP 1200a Typical Hardware Specifications cont.

Specification	DAP 1200a/4	DAP 1200a/6
Type of D⇒A Converter	Voltage Output	Voltage Output
Model of D⇒A Converter	Burr-Brown DAC813	Burr-Brown DAC813
Maximum Update Rate[3]	166K updates/sec	312K updates/sec
Number of Output Channels	2	2
Expandable To	66	66
Output Ranges	0 to 10 V -5 to 5 V -10 to 10 V	0 to 10 V -5 to 5 V -10 to 10 V
Resolution If Range is -5 to 5 volts	12 bits 2.4 mV	12 bits 2.4 mV
Accuracy If Range is -5 to 5 volts	±1 LSB, ±2.4 mV	±1 LSB, ±2.4 mV
Output Impedance	0.05 Ω	0.05 Ω
Current Source Maximum	±1 mA	±1 mA
Digital I/O Logic	FCT TTL	FCT TTL
Max. Digital Update Rate	166K words/sec	312K words/sec
Number of Input Bits Number of Output Bits	16 16	16 16
Expandable To	128 bits of input and 1024 bits of output	128 bits of input and 1024 bits of output
Digital Input Min. Logical High Max. Logical Low Max. Current Sink Max. Current Source	 2 V 0.8 V 20 µA 20 µA	 2 V 0.8 V 20 µA 20 µA
Digital Output Min. Logical High Max. Logical Low Max. Current Sink Max. Current Source	 2.6 V 0.5 V 24 mA 2.6 mA	 2.6 V 0.5 V 24 mA 2.6 mA
Hardware Clock Min. Pulse Width	25 ns	25 ns
Hardware Trigger Min. Pulse Width	60 ns	60 ns
Trigger Modes	GATED ONE-SHOT	GATED ONE-SHOT

[3] The DAP 1200a can update each of its two standard analog outputs at the specified maximum analog update rate. When analog output expansion is used, the update rate for expanded channels is determined by maximum digital update rate.

Expanded Analog Output Rate = Max. Digital Update Rate / (4 * Number of Channels)