e-Series Hardware Manual

Installation Guide and
Connector Reference

Version 4.50

Microstar Laboratories, Inc.

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1. Introduction

The Data Acquisition Processor is a complete data acquisition system which occupies one expansion slot in a personal computer. The Data Acquisition Processor combines analog data acquisition hardware with a 16-bit microprocessor, a large buffer memory, and a real-time multitasking operating system called DAPL. The Data Acquisition Processor handles all the low level details of data acquisition while performing computations in real-time. This frees the PC for user interaction and file management.

This Hardware Manual describes installation and use of Data Acquisition Processor hardware and hardware support products. Three other manuals complement the Hardware Manual.

- The Applications Manual introduces the Data Acquisition Processor by showing how to set up a wide variety of applications.
- The DAPL Manual describes the DAPL operating system which runs in the Data Acquisition Processor.
- The Systems Manual describes support software which runs in the PC, including support for writing programs in common programming languages.

For convenience, the DAPL Manual contains a merged index of all four Data Acquisition Processor manuals.

This manual describes four Data Acquisition Processor models: the DAP 800, the DAP 1200e, the DAP 2400e, and the DAP 3200e.

2. Installation and Checkout

This chapter describes Data Acquisition Processor hardware and software installation procedures for standard hardware configurations. Advanced installation options are found in Chapter 3.

Handling Precautions

Static control is required for handling all electronic equipment. The Data Acquisition Processor is especially sensitive to static discharge, however, because it contains many high-speed analog and digital components.

Observe the following precautions any time you handle the Data Acquisition Processor:

1. Wear a grounding strap during installation of the Data Acquisition Processor and at all other times when handling the Data Acquisition Processor. If it is not possible to use a grounding strap, continuously touching a metal screw on a grounded PC while handling the Data Acquisition Processor offers limited protection.

2. If it is necessary to transport the Data Acquisition Processor outside of the PC, be sure to shield the Data Acquisition Processor in a conductive plastic bag. If a conductive bag is not available, shield the Data Acquisition Processor by wrapping it completely in aluminum foil. Do not ship or store a Data Acquisition Processor in plastic peanuts without suitable shielding.

Static damage to analog components can cause subtle problems, including oscillation, increased settling time, and reduced slew rate. If you suspect that a Data Acquisition Processor has been affected by static discharge, return it to Microstar Laboratories for testing, repair, and quality control.

DOS Version

The Data Acquisition Processor requires version 3.0 or higher of DOS. Updates to the operating system are available from PC hardware distributors.

Getting Started

Before installing the Data Acquisition Processor software, make backup copies of all Microstar Laboratories diskettes and store the original diskettes in a safe place.

After making backup copies, insert Data Acquisition Processor diskette 1 in drive A and enter the DOS command

```
TYPE A:README.TXT |MORE
```

The PC will display any recent changes or corrections which are not included in the Data Acquisition Processor manuals.

The Data Acquisition Processor diskettes include a file named `FILES.TXT`; this file contains descriptions of all of the files on the diskettes.

Standard Configurations

The instructions in this chapter apply to PC systems containing only hardware options in the following list:

- diskette drive adapter
- color graphics adapter (CGA)
- monochrome display adapter
- enhanced graphics adapter (EGA)
- video graphics array (VGA)
- Hercules graphics adapter
- parallel printer adapter
- asynchronous communications adapter
- hard disk controller (PC/XT or PC/AT)
- memory expansion card
- game controller card

A PC/XT/AT/386/486 compatible computer which contains only these options is considered a standard configuration. Any system which contains an option not on this list is considered a nonstandard configuration. Users with nonstandard configurations should read the section ‘Nonstandard Configurations’ in Chapter 3 before proceeding.

Data Acquisition Processor Installation

The Data Acquisition Processor printed circuit board is compatible with AT/386/486 computers. The DAP 1200e, DAP 2400e, and DAP 3200e require 16 bit ISA slots. They also can fit in 32 bit EISA slots. The DAP 800 uses 8 bit PC/XT slots. It also can fit in 16 bit ISA slots and 32 bit EISA slots. To install the board, turn off the PC and insert the board into any free slot.

Note: Do not install the Data Acquisition Processor while the PC is turned on.

You must ensure that the PC's power supply has sufficient capacity for all of the expansion cards in your system. The Data Acquisition Processor requires approximately 15 Watts. If your system behaves erratically with the Data Acquisition Processor installed, you may need a larger power supply.

Software Installation

Before installing Data Acquisition Processor software, make backup copies of the Data Acquisition Processor diskettes. Put the original disks in a safe place, and use the backup disks as working copies.

The Microstar Laboratories INSTALL program installs the Data Acquisition Processor software on your system. To use INSTALL, boot your computer using DOS, place Data Acquisition Processor diskette 1 in drive `A`, and type the following command:

```
A:INSTALL
```

For systems with monochrome monitors, type:

```
A:INSTALL /BW
```

INSTALL prompts for configuration information including Data Acquisition Processor type and software destination directories. INSTALL provides information about each step to guide you through the installation process.

INSTALL copies several files to your boot disk and adds some information to your system configuration files. Your system configuration files are called `CONFIG.SYS` and `AUTOEXEC.BAT`. Backup copies of these files are created with the `.BAK` extension so that the original versions can be recovered if needed.

INSTALL also provides options for copying DAPview software and Data Acquisition Processor support software to your PC.

After running INSTALL, verify that software installation was successful by rebooting your PC. Before you see the DOS prompt, the following lines should appear on your screen:

```
ACCEL device driver 4.3
ACCEL driver initialization completed
DAPL initialization completed
```

The exact lines may vary slightly, depending upon configuration options. If a line is missing or if an error message appears, see the Troubleshooting section in this chapter.

When the DOS prompt is displayed, set the current directory to your DAPview directory and type the command:

```
DV
```

This command starts the DAPview program, allowing you to communicate interactively with the Data Acquisition Processor. Now everything you type at the PC keyboard is sent to the Data Acquisition Processor; all Data Acquisition Processor messages are printed on your screen. When the DAPview program begins, the following lines should be displayed on your screen:

```
*** DAPview [1.2] ***
*** DAPL Interpreter [4.4 XX/X] Serial# XXXXX ***
#
```

The appearance of the # prompt indicates that the Data Acquisition Processor is installed correctly. If the # prompt does not appear or if DAPview issues an error message and terminates, you have not established communication with the Data Acquisition Processor. Turn to the end of this chapter for troubleshooting hints.

Note: To exit from DAPview, press the Ctrl and Z keys simultaneously.

Once DAPview is communicating with the Data Acquisition Processor, you can type DAPL commands at your keyboard. The number sign (#) on the left side of your screen indicates that the Data Acquisition Processor is waiting for a command. At this time you can enter any of the sample applications from the Applications Manual. Running the examples in the Applications Manual is a good way to start learning how to use a Data Acquisition Processor.

Troubleshooting

The following are the errors which most commonly result from installation problems:

1. INSTALL prints an error message. Find the error message in the Systems Manual.

2. When your system is booted, the

```
ACCEL device driver 4.3
```

message is not printed. Check that the file `CONFIG.SYS` is present on your boot volume. If this file was not present before installation, it should have been placed on your boot volume by INSTALL. If the file `CONFIG.SYS` is present, check that it includes a line with the words

```
DEVICE=x:\yyy\ACOM.SYS ...
```

The "`x`" character should be the letter of your boot disk. "`yyy`" should be the correct directory where the file `ACOM.SYS` is located. If `CONFIG.SYS` is not on your boot volume, or if the `ACOM.SYS` line of the file `CONFIG.SYS` is incorrect, use the INSTALL program again, being careful to install the software on the correct volume.

3. If the message

```
Bad or missing ACOM.SYS
```

is printed, the file `ACOM.SYS` probably was not copied by INSTALL from the Data Acquisition Processor diskette to your boot volume. Use the INSTALL program again, being careful to install the software on the correct volume.

4. When your system is booted, one of the following messages is printed:

```
DAP hardware not found or improperly configured
DAP interrupt conflict
DAP interrupt selection error
```

These messages suggest a hardware conflict with another card in the PC; one or more of the Data Acquisition Processor configuration jumpers may need to be changed to resolve the conflict. See Chapter 3.

5. When your system is booted, the message

```
ACCEL driver initialization completed
```

is not printed. If an error message is printed by the ACOMINIT program, find the error message in the Systems Manual. If no error message is printed, check that the `AUTOEXEC.BAT` file on your boot volume contains a line beginning with the command ACOMINIT. If no ACOMINIT line is found, use the INSTALL program again, being careful to install the software on the correct volume.

6. The message

```
DAPL initialization completed
```

is not printed. If an error message is printed by the DAPLINIT program, find the error message in the Systems Manual. If no error message is printed, check that the `AUTOEXEC.BAT` file on your boot volume contains a line beginning with the command DAPLINIT. If no DAPLINIT line is found, use the INSTALL program again, being careful to install the software on the correct volume.

7. If DAPview prints the error message

```
Host communication port is uninitialized
```

then the file `CONFIG.SYS` was incorrect or missing at boot time. See #2.

8. If DAPview issues the error message

```
Could not establish communications
```

or if DAPview does not display a DAPL # prompt, the Data Acquisition Processor is not communicating with your PC. This may indicate that an error occurred at boot time. Check that no error messages are printed when you boot your system.

If your PC has cards other than those listed at the beginning of the chapter, a card may be interfering with communications. Remove optional cards, boot the PC, and try using DAPview again.

Check that the configuration jumpers on the Data Acquisition Processor are correct. These jumpers are labeled `HOST CONFIGURE` on the Data Acquisition Processor printed circuit board. See Chapter 3 for the correct jumper selections. Check also for consistency between the jumper settings on this connector and the settings on the `ACOM.SYS` line in the file `CONFIG.SYS`.

A final possibility is that the Data Acquisition Processor may be faulty. If you suspect that this is the case, call Microstar Laboratories Customer Support. When calling for installation support, please open your PC case so that the Data Acquisition Processor jumpers are visible, and be ready to provide the following information:

- the serial and model numbers of your Data Acquisition Processor.
- the contents of your AUTOEXEC.BAT and CONFIG.SYS files.
- a list of all hardware boards installed in your computer.

9. If your PC keyboard locks up when DAPview is started and does not accept the Ctrl-Z key, your PC may have an old style keyboard. Try starting DAPview with one of the following command line options:

```
DV /K1
DV /K2
```

10. If DAPview issues the error

```
Help file DV.HLP not found
```

check that the file DV.HLP has been copied to the directory containing the DAPview files. Check also to make sure the file AUTOEXEC.BAT has the line:

```
SET DV=C:\DV
```

Replace C:\DV with the name of the drive and directory containing the DV.HLP file.

3. Advanced Installation Options

Installation for standard hardware configurations is described in Chapter 2. This chapter covers installation in more detail.

Nonstandard Configurations

The Data Acquisition Processor uses two resources from the host PC:

- an interrupt vector
- a range of I/O addresses

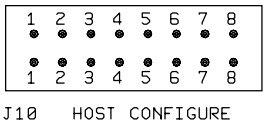
The Data Acquisition Processor allows several interrupt vector and I/O address selections. The interrupt vector may be 2, 3, 4, or 5. When selecting an interrupt vector, bear in mind the following interrupt vectors used by standard cards:

EGA/VGA	2
serial port COM2	3
serial port COM1	4
parallel port #2	5
hard disk controller on IBM XT	5
parallel port #1	7

The Data Acquisition Processor is shipped configured to use interrupt 2. EGA and VGA video adapters potentially can use interrupt 2, but most applications do not use this capability. Since interrupt 2 does not conflict with any other standard hardware, this is the default Data Acquisition Processor interrupt vector.

If any other cards are installed, determine the interrupts used and select a Data Acquisition Processor interrupt number distinct from these. Depending on the selection, the host computer may lose access to one of the serial `COM` ports or one of the parallel ports.

To change interrupt vectors, locate the sixteen pin `HOST CONFIGURE` connector:



J10 HOST CONFIGURE

This connector is directly above the gold fingers on the Data Acquisition Processor printed circuit board.

The following table gives the four possible interrupt selections:

Interrupt Vector	Jumper
2	pin pair 7
3	pin pair 4
4	pin pair 5
5	pin pair 6

To change the interrupt, remove the jumper and replace it according to this table. Note that exactly one of the pin pairs 4, 5, 6, and 7 should be connected.

When the interrupt is changed, the INSTALL program must be informed of the new interrupt selection. When running INSTALL, select the `DAP 0` button and select the interrupt number that matches the interrupt of the Data Acquisition Processor.

In addition to an interrupt vector, the other PC resource used by a Data Acquisition Processor is a range of I/O addresses. If nonstandard cards are used in the host PC, check that the Data Acquisition Processor I/O addresses do not conflict with those of the other cards. The Data Acquisition Processor is shipped configured to use I/O addresses in the range 220-22F (hexadecimal). This range may be changed by changing the jumpers on the `HOST CONFIGURE` connector. Pin pairs 1, 2, and 3 select the I/O address of the Data Acquisition Processor according to the following table:

I/O Address Range	Jumpers
220 - 22F	1,2,3
230 - 23F	2,3
240 - 24F	1,3
250 - 25F	3
320 - 32F	1,2
330 - 33F	2
340 - 34F	1

When the I/O address is changed, the INSTALL program must be informed of the new address selection. When running INSTALL, select the `DAP 0` button and select the address that matches the address of the Data Acquisition Processor.

Note: The only effect of changing the interrupt number or address in the INSTALL program is to change the value of the `/I` or `/A` parameter of the line `ACOM.SYS` that is inserted in the file `CONFIG.SYS`.

Voltage Range Selection

When shipped, the Data Acquisition Processor is configured for analog inputs and outputs in the range from -5 Volts to +5 Volts. Three other analog input ranges and two other analog output ranges are available. See the connector chapters for voltage range selection instructions.

Installing Several Data Acquisition Processors

Up to seven Data Acquisition Processor boards can operate simultaneously in one PC. Running several boards in parallel increases the maximum sampling rate and the real-time processing power of a system. For special options to install up to fourteen Data Acquisition Processor boards in one PC, contact Microstar Laboratories.

Each Data Acquisition Processor requires one PC slot. All the Data Acquisition Processors in a PC share just one interrupt line; no DMA lines are required. The Data Acquisition Processors are distinguished by their I/O addresses in the PC. Before installing Data Acquisition Processors in the PC, select a distinct I/O address for each board.

There are seven possible I/O addresses; this limits the number of Data Acquisition Processors in a PC to seven. Set the I/O addresses with the jumpers on the `HOST CONFIGURE` connector. See the connector chapters for more information about the `HOST CONFIGURE` connector.

Note: Pin pair 8 of the `HOST CONFIGURE` connector sets the level of the PC's interrupt line. Pin pair 8 must be connected for one Data Acquisition Processor in a PC, and must not be connected for all other Data Acquisition Processors.

INSTALL can perform installation for several Data Acquisition Processors. When typing the INSTALL command, add the option /Dx to the end of the command, where x is the number of boards. For example, the following line defines installation for three Data Acquisition Processors.

```
A:INSTALL /D3
```

INSTALL provides onscreen options for configuring each Data Acquisition Processor individually. Select a Data Acquisition Processor button to display a dialog box for choosing the Data Acquisition Processor model, address, and interrupt.

Note: The order in which the boards appear in the ACOM.SYS line in the file CONFIG.SYS determines the numbering of the Data Acquisition Processors. The first Data Acquisition Processor is DAP 0, the second is DAP 1, etc. The addresses do not matter when determining the numbering. When synchronous operation is used with DLOG, the last board in the list is the master unit.

The INSTALL Program

This section provides additional details about the INSTALL program. This information is only of interest to advanced Data Acquisition Processor users.

The INSTALL program installs Data Acquisition Processor software on a PC and configures the PC to initialize the ACCEL driver when the PC boots. INSTALL uses the following syntax:

```
A:INSTALL <options>
```

If installing from a drive other than A:, type the letter for that drive instead. INSTALL allows several command line options for special installation features. The following options are legal:

/Ix	use interrupt x
/DAPxxx:Ayyy	set Data Acquisition Processor type to xxx and set address to yyy
/Mxx	set ACCEL default mode to xx
/COMx	use serial port communication on com port x
/Dx	install x Data Acquisition Processors
/?	help

When running INSTALL, several prompts are provided for configuring Data Acquisition Processor software on a PC. Select a Data Acquisition Processor button to

choose the Data Acquisition Processor model, address, and interrupt for the Data Acquisition Processor. Choose the Select Software Options button to select the specific software options to install. For help on the options press F1.

After all options have been verified, INSTALL copies Data Acquisition Processor software to the PC and modifies the system files. INSTALL copies the files `ACOM.SYS`, `ACOMINIT.EXE`, `DAPLINIT`, and `Dx-x.STD` to the PC boot drive. INSTALL creates the file `ACOM.DAT` and places it on the boot drive. These files are all placed on the boot drive so they are available when the PC first boots.

After copying the boot files, INSTALL copies the software that was specified in the Select Software Options dialog box to the Main directory.

After copying files, INSTALL modifies two DOS configuration files.

INSTALL adds a line to the file `CONFIG.SYS` that loads the ACCEL device driver. If this line already exists from a previous installation, INSTALL replaces it. The following line is a typical line that INSTALL adds to `CONFIG.SYS`:

```
device=c:\dap\acom.sys i2 dap2400e:a220 m20 p19b
```

More information about the ACCEL driver configuration line is provided later in this chapter. If `CONFIG.SYS` does not exist, INSTALL creates it. Before modifying `CONFIG.SYS`, INSTALL saves an original copy in the file `CONFIG.BAK`.

INSTALL also modifies the file `AUTOEXEC.BAT` by adding several lines that configure the ACCEL driver with specific communication information. If these lines already exist from a previous installation, INSTALL replaces them. The following lines are typical lines that INSTALL adds to `AUTOEXEC.BAT`:

```
c:\dap\acominit c:\dap\acom.dat
@if errorlevel 1 pause
c:\dap\daplinit /reset c:\dap\d*.std
@if errorlevel 1 pause
```

The ACOMINIT program configures the ACCEL driver with specific communication pipe information provided by the file ACOM.DAT. For some Data Acquisition Processor models, the DAPLINIT program is required to initialize the DAPL operating system. More information about the ACOMINIT and DAPLINIT programs is provided later in this chapter. If AUTOEXEC.BAT does not exist, INSTALL creates it. Before modifying AUTOEXEC.BAT, INSTALL saves an original copy in the file AUTOEXEC.BAK.

Device Driver Configuration

This section explains the format of the device driver command that is placed in the CONFIG.SYS file by the INSTALL program. This information is of interest only to advanced programmers.

The format of the device driver command is:

```
DEVICE=ACOM.SYS [Ix] [DAP[yyy]:Azzz] [Muu] [Pwww]
```

Note: Several parameters are optional. The letters u through z in each parameter represent hexadecimal digits.

x specifies the interrupt vector that is used for PC communication. This number should match the configuration of jumper J10 on the Data Acquisition Processor.

The ACCEL driver automatically detects the type of Data Acquisition Processor that is installed. yyy is optional and manually specifies the board type. Valid names for the DAPyyy parameter are: DAP 800, DAP 801, DAP 1200e, DAP 2400, DAP 2400e, and DAP 3200e. Note that auto-detection should not be used with the DAP 801 because it may still be running after a PC warm boot. The INSTALL program enables auto-detection for all Data Acquisition Processors except the DAP 801.

zzz specifies the hexadecimal starting I/O address of the Data Acquisition Processor. This number must match the configuration of jumper J10 on the Data Acquisition Processor.

uu is a hexadecimal number that specifies the default mode of the ACCEL driver. See Chapter 13 of the Systems Manual for more information about ACCEL driver modes.

www is a hexadecimal number that specifies the number of paragraphs of memory to reserve for PC communications pipes. See the section ‘Com Pipe Configuration’ later in this chapter.

The following is a typical ACCEL driver command line:

```
device=c:\dap\acom.sys i2 dap:a220 m20 p19b
```

The ACCEL driver can be loaded into high memory with the DOS `devicehigh` statement. See your DOS manual for details on loading device drivers into high memory.

The ACOMINIT Program

ACOMINIT configures the ACCEL driver communication pipes. ACOMINIT is placed in the file `AUTOEXEC.BAT` to configure the ACCEL driver when the PC first boots. The syntax for ACOMINIT is:

```
ACOMINIT <cfg_file>
```

`<cfg_file>` provides communication pipe configuration information. `<cfg_file>` normally is named `ACOM.DAT`. The following section describes the contents of `ACOM.DAT`.

Com Pipe Configuration

This section describes the format of communication pipe configuration in the file `ACOM.DAT`. This information is not required for most applications. During initialization, the Microstar Laboratories program ACOMINIT reads the contents of a configuration file which specifies a com pipe configuration. The configuration file determines the connection between com pipes on the Data Acquisition Processor and com pipes on the PC. Lines in the configuration file have the following syntax:

```
<source> -> <destination> [<options>]
```

`<source>` and `<destination>` are specifications of communication pipe locations. A com pipe location is either a Data Acquisition Processor com pipe, a PC com pipe, or a PC serial port:

```
(DAP[n] CPIPE v)
(PC CPIPE w)
(SERIAL x)
```

`n` is the Data Acquisition Processor number when several boards are installed in one PC. `v` is a DAPL com pipe number. `w` is a PC com pipe number. `x` is a serial com pipe number. The space before `v, w,` and `x` can be omitted.

For example, the following lines connect the default text input and text output com pipes of the Data Acquisition Processor to the PC:

```
(dap cpipe 0) -> (pc cpipe 0)
(pc cpipe 0) -> (dap cpipe 0)
```

The first line connects DAPL output com pipe 0 to PC input com pipe 0. The second line connects PC output com pipe 0 to DAPL input com pipe 0. By default, DAPL defines two input com pipes and two output com pipes. Output com pipe 0, named `$SYSOUT`, is for text output to the PC. Output com pipe 1, named `$BINOUT`, is for binary output to the PC. Input com pipe 0, named `$SYSIN`, is for text input from the PC. Input com pipe 1, named `$BININ`, is for binary input from the PC.

Each line in the com pipe configuration file may contain one or more options, enclosed in square brackets. The following options are available:

```
BINARY
TEXT
MAXSIZE=xx
WIDTH BYTE | WORD | LONG
BINARY and TEXT specify the type of the data in the com
pipe. The default is TEXT.
```

`MAXSIZE` specifies the size of the PC buffer of the com pipe, in bytes. The default is 1024 bytes (256 bytes for the DAP 800). The INSTALL program sets the maximum size of the com pipes to be relatively small to conserve PC memory yet provide good performance. The Data Acquisition Processor automatically provides additional pipe buffering when needed. In some applications, increasing the maximum com pipe size can improve performance by allowing larger block operations. Performance can increase with com pipe sizes up to 4096 or 8192. Larger com pipe sizes typically do not provide further performance benefits.

`WIDTH` specifies the width of data items that are transferred through the com pipe. The `WIDTH` option must match the width of the corresponding Data Acquisition Processor com pipe. `BYTE` is the default for text com pipes and also is the only width allowed. `WORD` is the default for binary com pipes. Any width is allowed for binary com pipes.

The default com pipe configuration file generated by the INSTALL program is stored in the file `ACOM.DAT`. If the Data Acquisition Processor is operated inside a PC, the following configuration is placed in the file `ACOM.DAT`:

```
(dap0 cpipe0) -> (pc cpipe0) [text maxsize=1024]
(pc cpipe0) -> (dap0 cpipe0) [text maxsize=1024]
(dap0 cpipe1) -> (pc cpipe1) [binary maxsize=2048]
(pc cpipe1) -> (dap0 cpipe1) [binary maxsize=1024]
```

If the Data Acquisition Processor has a serial port and is operated in stand-alone mode (connected to the PC's `COM1` port), the following configuration is placed in the file `ACOM.DAT`:

```
(serial 1) -> (pc cpipe 0) [maxsize=256]
(pc cpipe 0) -> (serial 1) [maxsize=256]
```

Note: Only one of the two serial ports (`SERIAL1` and `SERIAL2`) can be used in a configuration file.

In some applications, additional com pipes need to be defined. More com pipes are needed when extra com pipes are defined in DAPL on a Data Acquisition Processor or when several Data Acquisition Processors are installed.

For special applications, extra com pipes can be defined in DAPL. See the `CPIPE` command in the DAPL Manual.

Note that in many cases, the commands `MERGE`, `MERGEF`, and `NMERGE` can be used instead of defining extra com pipes. It is best to use standard com pipes when possible to maintain a standard communication setup.

When more than one Data Acquisition Processor is installed in a system, additional com pipes need to be defined. For several Data Acquisition Processors , the following com pipe numbering is recommended:

```
DAP0
   system text pipe is PC com pipe #0
   system binary pipe is PC com pipe #1
DAP1
   system text pipe is PC com pipe #2
   system binary pipe is PC com pipe #3
DAP2
   system text pipe is PC com pipe #4
   system binary pipe is PC com pipe #5
.
.
DAP6
   system text pipe is PC com pipe #12
   system binary pipe is PC com pipe #13
```

P Parameter Size

In a system with additional com pipes, the memory available to the ACCEL driver must be increased. The `P` parameter in the `ACOM.SYS` line of the file `CONFIG.SYS` specifies the number of paragraphs of PC memory reserved for the ACCEL driver and com pipes. The storage requirement of the ACCEL driver and PC com pipes, in bytes, is:

```
Storage = 830 + (MaxSize in bytes) + (Number of com
   pipes)*190
```

`MaxSize in bytes` is the sum of all com pipe sizes defined in the file `ACOM.DAT`. `Number of com pipes` is the number of com pipes defined.

Note: This storage requirement applies for versions 4.32 and later of the ACCEL driver.

The `P` parameter is a hexadecimal number, specified in paragraphs. A paragraph of PC memory is 16 bytes. To determine the `P` parameter, divide the storage requirements by 16 and convert to hexadecimal.

The following example calculates the `P` parameter for the default `ACOM.DAT` file created by INSTALL. The result, in bytes, is divided by 16 to get the `P` parameter in paragraphs.

```
Storage = 830 + 5120 + 4*180 = 6710 bytes
P = 6710 / 16 = 420 paragraphs (decimal) = 1A4 (hex)
```

When defining additional com pipes, remember to define pipes for both the DAP-to-PC and PC-to-DAP direction. Some programs such as DAPview for Windows expect additional com pipes defined for both directions.

DAP to DAP Communication

Communication pipes can be configured to allow communication between two Data Acquisition Processors. DAP to DAP communication occurs over the PC bus in the background with no PC program intervention required. The following syntax is used in the file ACOM.DAT to configure DAP to DAP communication:

```
(DAPw CPIPEx) -> (DAPy CPIPEz)
(DAPy CPIPEz) -> (DAPw CPIPEx)
```

w is the number of the DAP that sends data. x is the Data Acquisition Processor communication pipe used to send data. y is the number of the Data Acquisition Processor that receives data. z is the Data Acquisition Processor communication pipe to receive data. The DAPL command CPIPE is needed to define the Data Acquisition Processor communication pipes on each Data Acquisition Processor.

The following example shows how to configure a system for DAP to DAP communication. This example configures two Data Acquisition Processors. DAP 0 samples one channel of data and sends the data to DAP 1 for analog output.

In the file ACOM.DAT, add:

```
(dap0 cpipe15) -> (dap1 cpipe15)     [binary maxsize = 1024]
(dap1 cpipe15) -> (dap0 cpipe15)     [binary maxsize = 1024]
```

DAP to DAP com pipes require twice the storage space as DAP to PC or PC to DAP com pipes. Fore the above DAP to DAP com pipe definition, the P parameter in CONFIG.SYS must be increased by 130 (hex). The following example calculates the P parameter increase:

```
storage increase = 2 * (2048 + 2 * 190) = 4856 (decimal)
P increase = 4856/16 = 304 paragraphs (decimal) = 130
  paragraphs (hex)
```

The following DAPL commands provide an example of how to implement DAP to DAP communication.

```
;  DAPL commands for DAP 0:

CPIPE TODAP1 PC NUM=15 OUTPUT BINARY WORD
RESET
IDEF A 1
   SET IPIPE0 S0
   TIME 10000
   END
PDEF B
   COPY(IPIPE0, TODAP1)
   END
START A,B


;  DAPL commands for DAP 1:

CPIPE FROMDAP0 PC NUM=15 INPUT BINARY WORD
RESET
PDEF A
   DACOUT(FROMDAP0, 0)
   END
START A
```

If a DAP 800 is receiving data from another Data Acquisition Processor, the receiving Data Acquisition Processor should be started first. Otherwise the communication pipes could fill up and lock out communication that is needed to send DAPL commands. e-Series boards do not have this restriction.

The DAPLINIT Program

DAPLINIT initializes the DAPL operating system on the Data Acquisition Processor by downloading a binary image of DAPL to the Data Acquisition Processor. ACCEL driver communication pipes must be configured using ACOMINIT before DAPLINIT is run. The syntax for DAPLINIT is as follows:

```
DAPLINIT [/RESET] [<dapl_file>] [<dapl_file>]*
```

`<dapl_file>` specifies a binary file containing DAPL. DAPLINIT allows several DAPL binary files on the command line to initialize several Data Acquisition Processors in a PC.

The optional parameter /RESET requests a hardware reset of the Data Acquisition Processor before downloading DAPL. If /RESET is not specified, all Data Acquisition Processors retain their state during a warm PC boot.

DAPLINIT detects the Data Acquisition Processor model types on the ACOM.SYS line of the file CONFIG.SYS. DAPLINIT downloads the DAPL files, in order, to the Data Acquisition Processors that require DAPL initialization.

DAPLINIT can accept a wildcard file specification to allow flexibility for when Data Acquisition Processor installations change. With a wildcard file name, DAPLINIT searches the current directory and the DOS PATH to find a DAPL binary file that matches the Data Acquisition Processor type that is installed. The following example shows how DAPLINIT can be configured to search for the correct DAPL/STANDARD binary file.

```
DAPLINIT /RESET D*.STD
```

The INSTALL program automatically configures new installations to use a wildcard file name for DAPLINIT.

Installation on a Network

Data Acquisition Processor software can be installed on a network consisting of PC workstations connected to one or more servers. The INSTALL program can copy Data Acquisition Processor software to a PC workstation from a network that has a copy of the Data Acquisition Processor software disk image.

Note: When using Data Acquisition Processor software on a network, each simultaneous user must have a licensed copy of the software.

When installing Data Acquisition Processor software from a network, INSTALL copies several files to the PC workstation boot drive. The files are ACOM.SYS, ACOMINIT.EXE, ACOM.DAT, and, if necessary, DAPLINIT.EXE and Dx-x.STD. These files must be on the PC boot drive so that they are available immediately at boot time. INSTALL copies the remaining Data Acquisition Processor software to a network drive for use once the network is connected. INSTALL modifies AUTOEXEC.BAT and CONFIG.SYS on the workstation boot drive as in regular installations.

DAPL Licensing

When a Data Acquisition Processor is shipped from the factory, a copy of DAPL is provided that is licensed to run on the Data Acquisition Processor. When a Data Acquisition Processor software upgrade is shipped, the DAPL file on the upgrade is licensed to be used with the Data Acquisition Processor that was specified when the upgrade was ordered.

Removing Data Acquisition Processor Software

When a Data Acquisition Processor is removed from a PC, the software can be removed as well. This section describes how to remove a Data Acquisition Processor software installation.

1. Delete the directory where Data Acquisition Processor software was installed. Usually this directory is `c:\dap`. Delete all the subdirectories under the Data Acquisition Processor directory. Make sure that there are no important data files in these directories before deleting them.

2. Edit the file `AUTOEXEC.BAT`. Delete the following four lines:

```
c:\dap\acominit c:\dap\acom.dat
@if errorlevel 1 pause
c:\dap\daplinit /reset c:\dap\d*.std
@if errorlevel 1 pause
```

3. Edit the file `CONFIG.SYS`. Delete the following line:

```
device=c:\dap\acom.sys i2 dap:a220 m20 p19b
```

4. DAP 800 Connectors

This chapter discusses the interface connectors on the DAP 800 and DAP 801. Descriptions of the DAP 800 include the DAP 801 unless stated otherwise. Figure 1 shows component placement outlines of the DAP 800. The only components shown are connectors, whose labels begin with the letter J, and some integrated circuits, whose labels begin with the letter U.

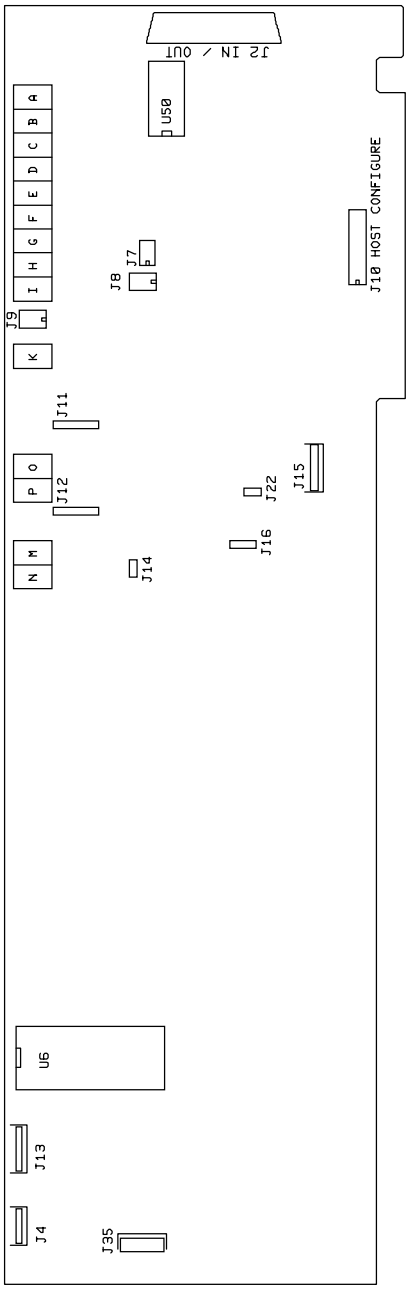
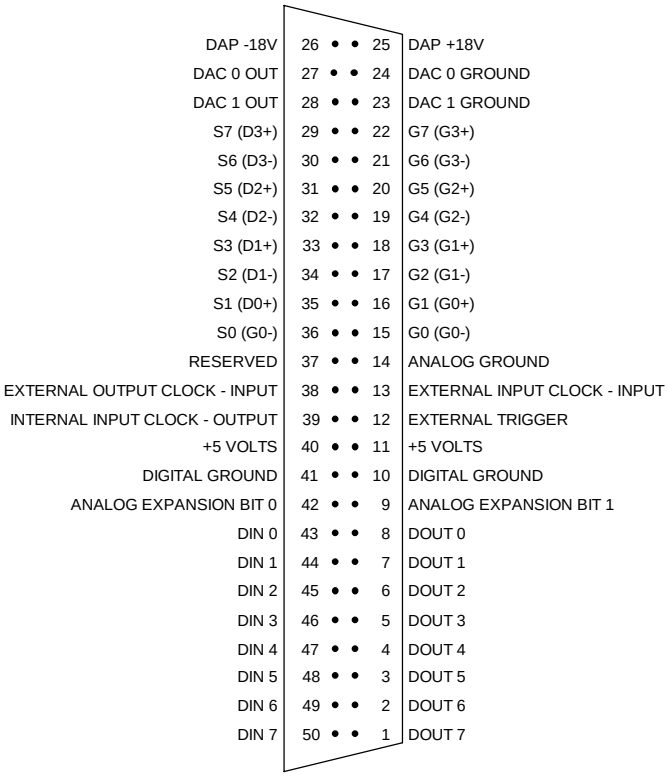


Figure 1.
DAP 800

Input/Output Connector

Analog and digital voltages are connected to the Data Acquisition Processor through a 50 pin connector on the back panel of the PC. This connector is located on the right side of the Data Acquisition Processor and is labeled `J2 IN/OUT`. It has a double row of pins on 0.050 inch centers. The connector is AMP part number 749649-5. It mates with discrete wire connector T&B part number HFM050A or insulation displacement connector AMP part number 786090-5. J2 mates with cable part numbers MSCBL 047-01, MSCBL 048-01, MSCBL 049-01K, MSCBL 050-01, and MSCBL 051-01K.

Looking at the input/output connector from the back of a PC, the pin numbering is:



Note: Use the pin numbering on this chart, rather than numbers which may be found on your connector. Connectors from different manufacturers are not numbered consistently.

Single-ended analog inputs are shown as S0 through S7 and ground inputs are shown as G0 through G7. Differential analog inputs are shown as D0- and D0+ through D3- and D3+, their corresponding ground inputs are G0- and G0+ through G3- and G3+.

Digital inputs are indicated by DIN 0-7 and digital outputs are indicated by DOUT 0-7. Bit 0 is the least significant bit.

Digital-to-analog outputs are indicated by DAC0 and DAC1. Their corresponding ground inputs are DAC0 GROUND and DAC1 GROUND.

Pin 13 is the external clock input and pin 39 is the internal clock output. Pin 12 is the external trigger connection. Pin 38 is the external output clock input.

Pins 11 and 40 are connected to the 5 volt digital power supply. Pins 25 and 26 are +18 volt and -18 volt supplies respectively.

Pin 37 is reserved and should not be used.

A termination board to connect all lines of the input/output connector to discrete wire connectors is available from Microstar Laboratories.

The following sections describe the input/output connector pins in greater detail.

Analog Input

Analog voltages are connected to the DAP 800 through the 50 pin input/output connector on the back panel of the PC.

Single-ended analog inputs are indicated by S0 through S7; their corresponding ground inputs are G0 through G7. Differential inputs are indicated by D0- and D0+ through D3- and D3+; their corresponding ground inputs are G0- and G0+ through G3- and G3+.

A single-ended analog signal should be connected to an analog input pin and to the adjacent analog ground pin, for example to pins 36 and 15. A differential analog signal should be connected to two adjacent analog input pins and to either of their corresponding grounds, for example to input pins 36 and 35, and ground pin 15 or ground pin 16.

Analog input signals should be within the range from -10 volts to +10 volts, relative to the ground of the Data Acquisition Processor. The DAP 800 is provided with fault-protected input multiplexers. The analog inputs are protected against voltages up to +/- 25 volts. Input signals may be applied to the DAP 800 when the PC's power is off.

Analog Output

The input/output connector on the DAP 800 includes digital-to-analog converter outputs. Pins 27 and 28 are the outputs of `DAC0` and `DAC1`, respectively. Pins 24 and 23 are the corresponding grounds. The digital-to-analog converters have voltage outputs with typical output impedances of 2 Ohms. These normally should drive high impedance inputs. The output current from each digital-to-analog converter output is rated at ±5 milliamps but it is recommended that this current not exceed ±1 milliamp.

Analog outputs are set to zero when the system is first powered on. When analog outputs are configured for unipolar mode, the outputs are set to half of the full scale range when the system is first powered on.

Digital Input/Output

Digital input and output pins are located on the input/output connector on the back panel of the PC.

Digital inputs are indicated by `DIN 0-7` and digital outputs are indicated by `DOUT 0-7`. Bit 0 is the least significant bit.

The digital inputs are FCT TTL; they sink no more than 20 microamps for a “1” input and source no more than 0.2 milliamps for a “0” input. An input voltage greater than 2V is interpreted as a “1” and an input voltage less than 0.8V is interpreted as a “0”. Each digital input has a 10 KOhm resistor to +5 volts.

Digital inputs may have signals applied when the Data Acquisition Processor is off.

Digital outputs are set to "0" when the system is first powered on. The digital outputs are FCT TTL; they can sink no more than 24 milliamps for a “0” output and can

source no more than 2.6 milliamps for a “1” output. The output voltage for a “1” is at least 2.6V and the output voltage for a “0” is at most 0.5V.

External Clock and Trigger

The input/output connector on the DAP 800 includes connections for internal clock output, external clock input, and external trigger input.

The external input clock - input pin is used to connect an external input clock to the DAP 800. The internal input clock - output pin is the buffered output of the DAP 800 input clock circuit.

Pin 12 is an external trigger connection. The external trigger for the DAP 800 is either one-shot or gated, depending on the `HTRIGGER` command in the active input procedure. The external trigger of the DAP 800 is ignored if there is no `HTRIGGER` command in the active input procedure.

An external trigger signal must be within the standard TTL logic range of 0 to +5 volts. The Data Acquisition Processor provides a pull-up resistor on the external trigger input. This forces the trigger input active if it is left unconnected.

Clock and trigger inputs may have signals applied when the Data Acquisition Processor is off.

See Chapter 8 for more information about the external clock and the trigger.

Supply Voltages

The input/output connector provides connections to DAP 800 supply voltages. Pins 25 and 26 are connected to +18 volt and -18 volt analog supplies. These supplies can be used for low current, low noise devices such as external multiplexers. The maximum allowable current drain from these supplies is 25 milliamps per side. If more current than this is required, either use an external supply or use the 5 volt digital power supply found on pins 11 and 40. The 5V supply is rated at 500 milliamps per connection. Note that this supply is unregulated.

Shunts

Several of the Data Acquisition Processor options are set by shunts. These are jumper wires enclosed in plastic, designed for connecting pins on 0.100" centers.

Each shunt has a top and a bottom. When a shunt is placed correctly, a probe point is visible in the shunt. Shunts must not be placed upside down on the pins, as incorrectly placed shunts do not provide reliable contacts.

Analog Signal Path Selection

In addition to the DAPL configuration options, the Data Acquisition Processor has several hardware configuration options. These determine the path taken by analog signals from the input pins to the analog-to-digital converter.

The analog signal path between the input pins and the analog-to-digital converter consists of the following functional units:

1. input multiplexers
2. instrumentation amplifier
3. programmable gain amplifier
4. bipolar offset circuit
5. analog-to-digital converter with sample and hold amplifier

Analog signals must pass through the input multiplexers, the instrumentation amplifier, and the analog-to-digital converter. Jumpers determine whether the analog signal path includes the programmable gain amplifier and the bipolar offset circuit, and also determine the input voltage range.

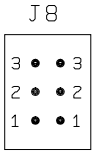
A signal range is called bipolar if it includes both positive and negative voltages; a signal range is called unipolar if it includes voltages of only one sign. The bipolar

offset circuit allows the analog-to-digital converter to operate with bipolar voltages. Jumpers select from three bipolar ranges and one unipolar range. If the programmable gain amplifier is enabled, gains of 1, 10, 100, and 1,000 are software selectable.

Analog Signal Path Selection Connectors

The following connectors control the analog signal path of the DAP 800. Note that changing voltage ranges may require recalibration.

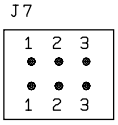
The input signal to the DAP 800 sample and hold amplifier is selected by J8, a header of two rows on 0.100 inch centers.



Exactly one jumper should be placed on J8, as follows:

Jumper	Signal range
1	bipolar
2	unipolar, gain enabled
3	unipolar, gain disabled

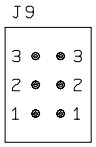
The input signal to the DAP 800 bipolar offset circuit is selected by J7, a header of two rows on 0.100 inch centers.



Exactly one jumper should be placed on J7, as follows:

Jumper	Signal range
1	unipolar
2	bipolar, gain enabled
3	bipolar, gain disabled

The DAP 800 bipolar voltage range is selected by J9, a header of two columns on 0.100 inch centers.



Exactly one jumper should be placed on J9, as follows:

Jumper	Bipolar range
1	-10 volts to +10 volts
2	-5.0 volts to +5.0 volts
3	-2.5 volts to +2.5 volts

Note: Differential signals may range from -10 volts to +10 volts, regardless of the input voltage range.

For the DAP 800, connector J14, located below the digital-to-analog converters, also must be set to specify whether the input voltages are unipolar or bipolar. A jumper must be placed across the pins of J14 for bipolar inputs; the jumper must be omitted for unipolar inputs.

The following table summarizes the DAP 800 jumper connections:

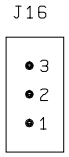
ADC Range	J7	J8	J9	J14
0v to 5v	1	2	Don't care	Off
±2.5v	2	1	3	On
±5v *	2 *	1 *	2 *	On *
±10v	2	1	1	On

* Factory Configuration

Channel List Selection

The DAP 800 has two possible external input clocking modes. When Channel List Clocking is enabled, all input pins are sampled on each low to high transition of the external clock. When Channel List Clocking is disabled, a single pin is sampled on each low to high transition of the external clock. See Chapter 8 for more details.

Connector `J16`, located near the center of the DAP 800, determines the clocking mode for external clocking. `J16` is a three pin vertical header of one column on 0.100 inch centers. The factory configuration is “enabled.”

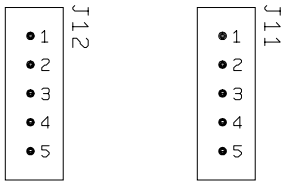


Exactly one jumper should be placed on `J16`, as follows:

Pins	Channel List Clocking
2,3	disabled
1,2	enabled

Analog Output Voltage Range Selection

The voltage ranges of `DAC0` and `DAC1` are selected by headers `J11` and `J12`, respectively:



One or two jumpers should be placed on `J11` and `J12`, as follows:

Jumpers	Range
1 to 2, 4 to 5	0 volts to +10 volts
2 to 3, 4 to 5	-5 volts to +5 volts
2 to 3	-10 volts to +10 volts

By default, DAPL assumes that the outputs of the digital-to-analog converters are bipolar. If a unipolar output range is selected, the following DAPL command must be issued:

```
OPTION BPOUTPUT=OFF
```

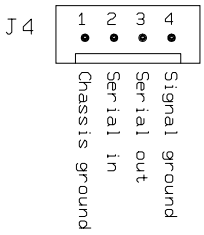
The following table summarizes the DAP 800 output jumper connections:

Voltage Range	J11/DAC0	J12/DAC1
0v to 10v	1-2, 4-5	1-2, 4-5
±5v *	2-3, 4-5 *	2-3, 4-5 *
±10v	2-3	2-3

* Factory Configuration

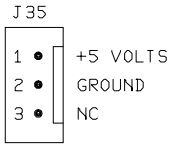
Serial Connector, DAP 801

On a DAP 801, the serial connector J4 has a single row of pins on 0.100 inch centers, located at the upper left of the Data Acquisition Processor printed circuit board. The connector is Molex part number 22-23-2041. It mates with Molex crimp terminal connector 22-01-3047. Serial cables can be ordered from Microstar Laboratories. The MSCBL010-01 is a printer-compatible serial cable and the MSCBL013-01 is a PC-compatible serial cable. Voltage levels on the serial connector conform to the RS-232 standard.



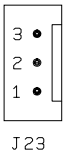
External Power Connector, DAP 801

On a DAP 801, the external power connector J35 has a single row of pins on 0.156 inch centers and is located near the left side of the Data Acquisition Processor printed circuit board. The connector is Molex part number 26-60-4030. It mates with Molex connector 09-50-3031. The DAP 801 requires +5 Volts at 2 Amps.



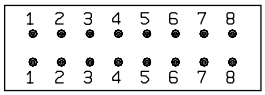
Reset Activation Header, DAP 801

In its standard configuration, the DAP 801 is reset automatically when power is applied. This automatic power-up reset is required for stand-alone operation. In this configuration, DAPLINIT software resets are ignored. When a DAP 801 is used inside a PC, DAPLINIT software resets can be enabled by placing a jumper across pins 1 and 2 of jumper J23. Pins 1 and 2 are the lower two pins of jumper J23. J23 is located just below J15 and to the left of the PC bus connector.



Host Configuration Connector

This connector is directly above the gold fingers on the Data Acquisition Processor printed circuit board.



J10 HOST CONFIGURE

Pin pairs 1, 2, and 3 select the I/O address of the Data Acquisition Processor according to the following table:

I/O Address Range	Jumpers
220 - 22F	1,2,3
230 - 23F	2,3
240 - 24F	1,3
250 - 25F	3
320 - 32F	1,2
330 - 33F	2
340 - 34F	1
deselect	none

Pin pairs 4 through 7 select the PC interrupt vector used for communications:

Interrupt Vector	Jumper
2	pin pair 7
3	pin pair 4
4	pin pair 5
5	pin pair 6

A jumper should be connected across exactly one pin pair.

A jumper always should be connected across pin pair 8 for one board in a system. This jumper is provided to allow for several Data Acquisition Processors in one PC. In these systems, exactly one Data Acquisition Processor should have this jumper installed.

Synchronization Connector

The synchronization connector J13 has a single row of pins on 0.100 inch centers. J13 is located at the upper left of the Data Acquisition Processor printed circuit board. The

synchronization connector allows several Data Acquisition Processors to share the same sampling clock. See Chapter 20 of the Systems Manual for more information about using synchronous Data Acquisition Processors.

For synchronization, the shared sampling clock requires special cabling between Data Acquisition Processors. For DAP 800's, the analog sampling clock of the master unit is supplied to the slave units by means of the cable MSCBL 015-01. Contact Microstar Laboratories for more information about cabling for synchronous Data Acquisition Processors.

5. DAP 1200e and DAP 2400e Connectors

This chapter discusses the interface connectors on the DAP 1200e and the DAP 2400e. Figure 2 and Figure 3 show component placement outlines of the DAP 1200e and the DAP 2400e. The only components shown are connectors, whose labels begin with the letter J, some integrated circuits, whose labels begin with the letter U, and trim potentiometers, whose labels are single letters.

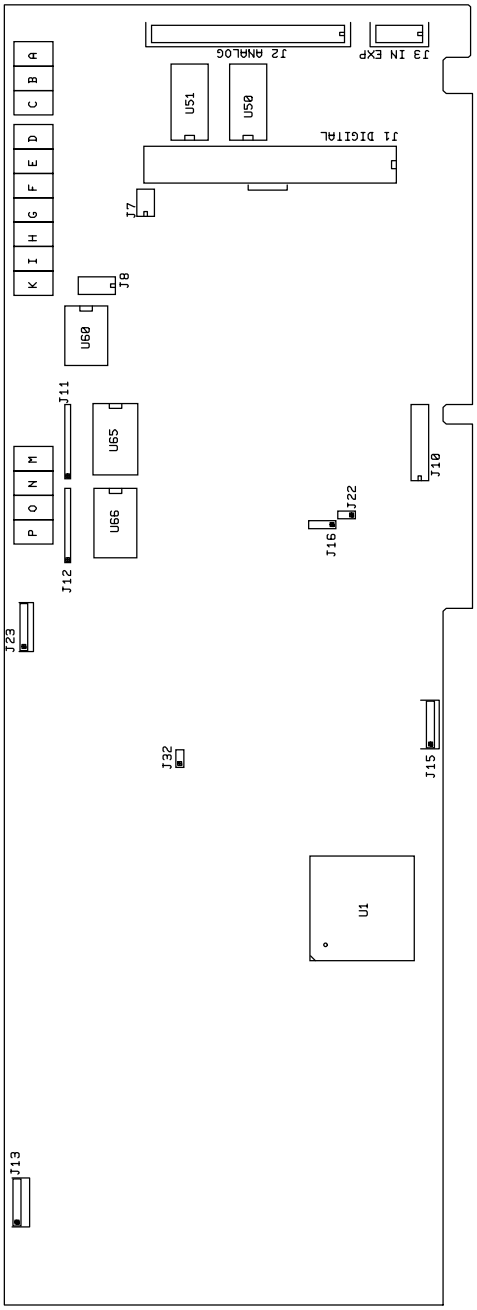


Figure 2.
DAP 1200e

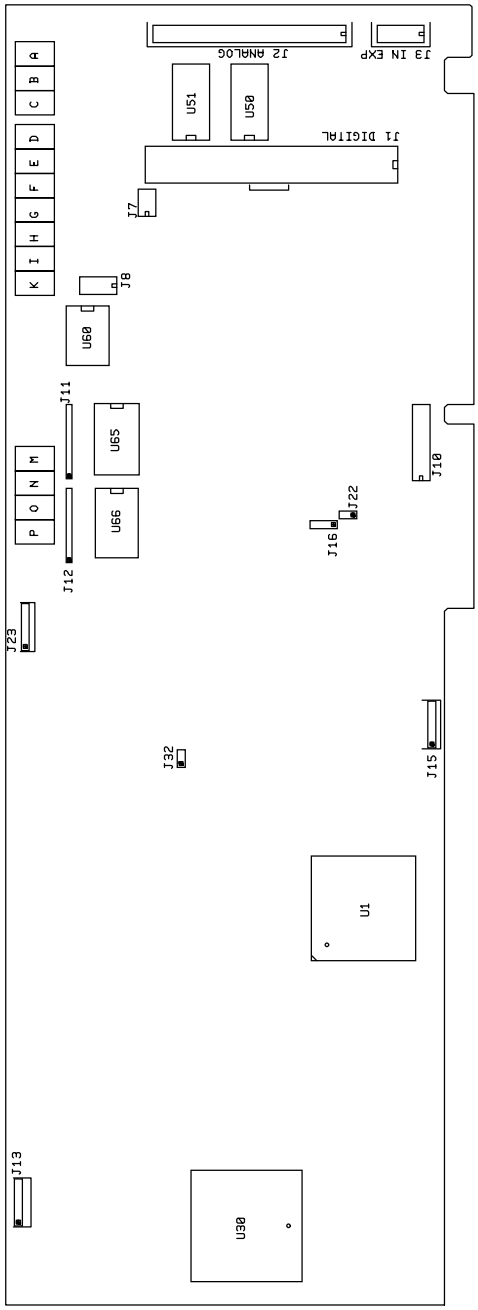
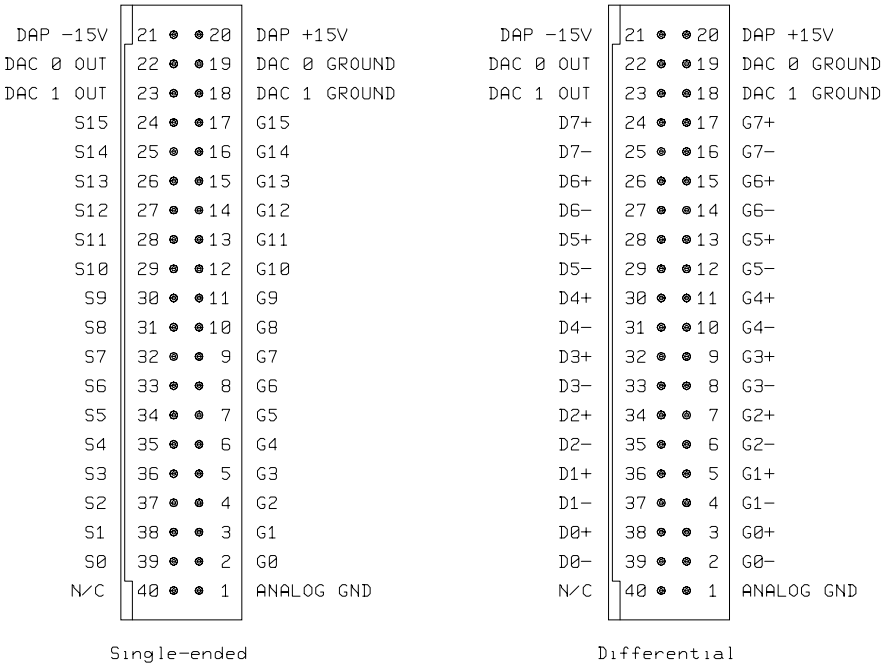


Figure 3.
DAP 2400e

Analog Input/Output Connector

Analog voltages are connected to the Data Acquisition Processor through a 40-pin analog connector on the back panel of the PC. This connector is located on the right side of the Data Acquisition Processor and is labeled `ANALOG IN/OUT`. It has a double row of pins on 0.100 inch centers. The connector is AMP part number 87476-6. It mates with discrete wire connector AMP 3-87631-6 or insulation displacement connector AMP 499954-8.

Looking at the analog connector from the back of a PC, the pin numbering is:



Note: Use the pin numbering on this chart, rather than numbers which may be found on your connector. Connectors from different manufacturers are not numbered consistently.

Single-ended inputs are indicated by S0 through S15; their corresponding ground inputs are G0 through G15. Differential inputs are indicated by D0- and D0+ through D7- and D7+; their corresponding ground inputs are G0- and G0+ through G7- and G7+. Every differential signal must be referenced to the corresponding ground. Data Acquisition Processors have a limited common mode voltage range and a ground connection must be used to assure that this range is not exceeded.

A single-ended analog signal should be connected to an analog ground pin and to an analog input pin, for example to pins 2 and 39. A differential analog signal should be connected to two adjacent analog input pins and either of their corresponding grounds, for example to input pins 39, 38, and ground pin 2 or 3.

Termination boards to connect all lines of the analog connector to discrete wire connectors are available from Microstar Laboratories.

The DAP 1200e and DAP 2400e are available either with standard input multiplexers or with fault-protected input multiplexers. Fault-protected input multiplexers also are available from Microstar Laboratories.

Analog input signals should be within the range from -10 volts to +10 volts, relative to the ground of the Data Acquisition Processor. With standard input multiplexers, analog input signals should not be applied to the Data Acquisition Processor when the PC's power is off. With fault-protected input multiplexers, input signals may be applied to the Data Acquisition Processor when the PC's power is off. Fault-protected multiplexers protect against voltages up to +/- 25 volts, but reduce the maximum sampling speed slightly. See Chapter 7 for electrical characteristics of the analog input pins.

The analog connector of the Data Acquisition Processor includes digital-to-analog converter output pins and analog supply voltages. Pins 22 and 23 are the outputs of DAC0 and DAC1, respectively. Pins 19 and 18 are the grounds for DAC0 and DAC1, respectively. The digital-to-analog converters have voltage outputs with typical output impedance of 0.2 Ohms. These normally should drive high impedance inputs. The output current from each digital-to-analog converter output is rated at ±5 milliamps, but it is recommended that this current not exceed ±1 milliamp.

Analog outputs are set to zero when the system is first powered on. When analog outputs are configured for unipolar mode, the outputs are set to half of the full scale range when the system is first powered on. When J32 is removed, the analog outputs at power-on may vary by up to 5 millivolts.

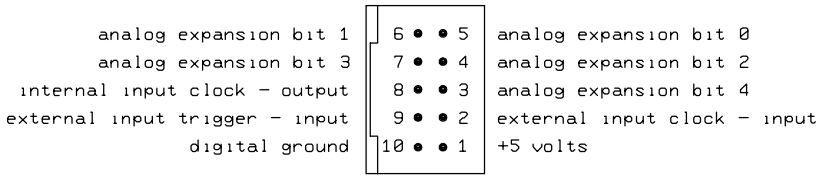
Pin 1 is analog power ground. Pins 20 and 21 are connected to +15 volt and -15 volt analog supplies. The maximum allowable current drain from these supplies is 50 milliamps per side. These supplies can be used for low current, low noise devices such as external multiplexers. To supply power to other devices, either use an external supply or use the 5 volt digital power supply found on the analog control connector with an external DC-to-DC converter.

Analog Control Connector

The analog control connector provides analog input expansion control lines, an external trigger input, an external input clock input, an internal input clock output, and connections to the 5 volt digital supply and its ground. The analog control connector is on the edge of the Data Acquisition Processor, directly below the analog input/output connector. It has two rows of five pins on 0.100 inch centers.

The analog control connector is manufactured by AMP, part number 102570-3. It mates with AMP insulation displacement connector 499499-1 for connection to a ribbon cable or AMP connector 87922-1 for connection to discrete wires.

The DAP 1200e and DAP2400e analog control connector, as seen from the back of a PC, has the following pin numbering:



Pins 3 - 7 provide TTL-compatible analog input expansion control signals that select the expansion port. The five highest order bits of the input pin number appear in descending order on pins 3, 7, 4, 6, and 5 for a period starting one sample time before the analog input is sampled.

External analog input expansion boards are available from Microstar Laboratories. Each input expansion board allows up to 32 differential inputs, or up to 64 single-ended inputs, or any combination requiring up to 64 input lines. A Data Acquisition Processor can control up to 8 external expansion boards in parallel, for a total of 512 input lines. See Chapter 13 for more information.

The analog control connector has an input pin for an active high external trigger. The external input trigger can be used to control when input sampling occurs. To use the external trigger, an `HTRIGGER` command is needed in the active input procedure. The

external trigger is ignored if there is no HTRIGGER command in the active input procedure. See Chapter 8 for more information.

An external trigger signal must be within the standard TTL logic range of 0 to +5 volts. The Data Acquisition Processor provides a pull-up resistor on the external trigger input. This forces the trigger input active if it is left unconnected.

Clock and trigger inputs may have signals applied when the Data Acquisition Processor is off.

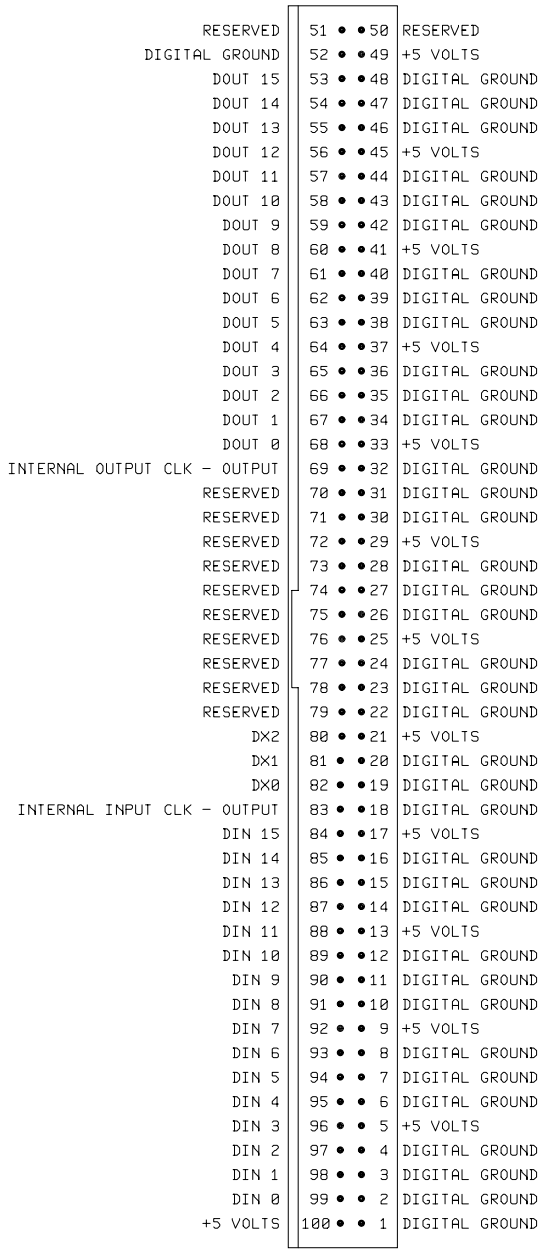
The analog control connector has input and output pins for an external input clock. The input pin should be used to connect an external input clock. The output pin is the buffered output of the internal clock circuit. See Chapter 8 for more information.

Pin 1 provides +5 volt power. Maximum current from this pin is 1 Amp.

Digital Input/Output Connector

The digital input/output connector is a vertical 100-pin connector labeled DIGITAL IN/OUT. This connector is near the right edge of the Data Acquisition Processor printed circuit board, to the left of the analog input/output connector. Note that this connector is not accessible from the back of the PC. The digital connector has two rows of 50 pins on 0.050 inch centers. The standard connector is manufactured by AMP, part number 1-104549-0. The digital input/output connector mates with insulation displacement connector AMP 1-111196-6.

The pin numbering of the digital input/output connector is shown in the following diagram:


RESERVED 51 • • 50 RESERVED
DIGITAL GROUND 52 • • 49 +5 VOLTS
DOUT 15 53 • • 48 DIGITAL GROUND
DOUT 14 54 • • 47 DIGITAL GROUND
DOUT 13 55 • • 46 DIGITAL GROUND
DOUT 12 56 • • 45 +5 VOLTS
DOUT 11 57 • • 44 DIGITAL GROUND
DOUT 10 58 • • 43 DIGITAL GROUND
DOUT 9 59 • • 42 DIGITAL GROUND
DOUT 8 60 • • 41 +5 VOLTS
DOUT 7 61 • • 40 DIGITAL GROUND
DOUT 6 62 • • 39 DIGITAL GROUND
DOUT 5 63 • • 38 DIGITAL GROUND
DOUT 4 64 • • 37 +5 VOLTS
DOUT 3 65 • • 36 DIGITAL GROUND
DOUT 2 66 • • 35 DIGITAL GROUND
DOUT 1 67 • • 34 DIGITAL GROUND
DOUT 0 68 • • 33 +5 VOLTS
INTERNAL OUTPUT CLK – OUTPUT 69 • • 32 DIGITAL GROUND
RESERVED 70 • • 31 DIGITAL GROUND
RESERVED 71 • • 30 DIGITAL GROUND
RESERVED 72 • • 29 +5 VOLTS
RESERVED 73 • • 28 DIGITAL GROUND
RESERVED 74 • • 27 DIGITAL GROUND
RESERVED 75 • • 26 DIGITAL GROUND
RESERVED 76 • • 25 +5 VOLTS
RESERVED 77 • • 24 DIGITAL GROUND
RESERVED 78 • • 23 DIGITAL GROUND
RESERVED 79 • • 22 DIGITAL GROUND
DX2 80 • • 21 +5 VOLTS
DX1 81 • • 20 DIGITAL GROUND
DX0 82 • • 19 DIGITAL GROUND
INTERNAL INPUT CLK – OUTPUT 83 • • 18 DIGITAL GROUND
DIN 15 84 • • 17 +5 VOLTS
DIN 14 85 • • 16 DIGITAL GROUND
DIN 13 86 • • 15 DIGITAL GROUND
DIN 12 87 • • 14 DIGITAL GROUND
DIN 11 88 • • 13 +5 VOLTS
DIN 10 89 • • 12 DIGITAL GROUND
DIN 9 90 • • 11 DIGITAL GROUND
DIN 8 91 • • 10 DIGITAL GROUND
DIN 7 92 • • 9 +5 VOLTS
DIN 6 93 • • 8 DIGITAL GROUND
DIN 5 94 • • 7 DIGITAL GROUND
DIN 4 95 • • 6 DIGITAL GROUND
DIN 3 96 • • 5 +5 VOLTS
DIN 2 97 • • 4 DIGITAL GROUND
DIN 1 98 • • 3 DIGITAL GROUND
DIN 0 99 • • 2 DIGITAL GROUND
+5 VOLTS 100 • • 1 DIGITAL GROUND

Pins 1 and 100 are closest to the gold edge fingers.

Digital inputs are indicated by `DIN 0-15` and digital outputs are indicated by `DOUT 0-15`. Bit 0 is the least significant bit.

A termination board from Microstar Laboratories, part number MSTB 008-01, connects all lines of the digital connector to discrete wire connectors.

The digital inputs are ALS TTL; they sink no more than 20 microamps for a “1” input and source no more than 0.2 milliamps for a “0” input. An input voltage greater than 2V is interpreted as a “1” and an input voltage less than 0.8V is interpreted as a “0”. The digital input lines have 10K pull-up resistors. When no signal is connected, a digital input is read as a “1.”

Digital inputs may have TTL signals applied when the Data Acquisition Processor is off.

Digital output polarity at power-on is selected by the Digital Output Reset Polarity Jumper described later in this chapter.

The digital outputs are ALS TTL; they can sink no more than 24 milliamps for a “0” output and can source no more than 2.6 milliamps for a “1” output. The output voltage for a “1” is at least 2.4V and the output voltage for a “0” is less than 0.5V.

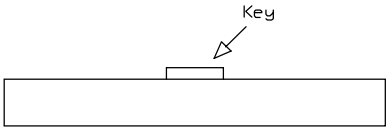
The digital input/output connector has multiple connections for the Data Acquisition Processor +5V power supply. The supply current is rated at 500 milliamps per connection with a total current limit of 2 Amps. The 2 Amp current limit is due to the limited current available from the host computer.

Pins 80, 81, and 82 provide TTL-compatible digital input expansion control signals. The low-order bit of the port number appears on pin 82, the middle bit appears on pin 81, and the high-order bit appears on pin 80.

An optional digital input port may be specified in a DAPL `SET` command. The digital input port numbers should range from 0 to 7. The specified port number appears on the control pins for a period starting one sample time before the time at which the digital inputs are sampled. The port number can be used to control external multiplexers.

An external digital expansion board is available from Microstar Laboratories. Each external expansion board allows up to 64 digital inputs and 64 digital outputs. See Chapter 16 for more information.

The Microstar Laboratories cable MSCBL 036-01 is compatible with the digital input/output port. The diagram below shows the key on the cable MSCBL 036-01. This key must be towards the left side of the Data Acquisition Processor.



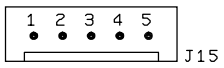
Note: Cables not made by Microstar Laboratories may have different keys.

Output Clock Connector

Connector `J15` is a five-pin connector, Molex part number 22-23-2051; the mating connector is Molex part number 22-01-3057. `J15` is located on the lower edge of the Data Acquisition Processor, between the 80186 CPU and the gold edge fingers.

The output clock signals and the output trigger signal are on connector `J15`, along with power and ground. These signal pins can be used to control when outputs are updated. See Chapter 8 for more details.

The pin numbering for `J15` is given in the following table:




```
Pin 1  Ground
Pin 2  External output trigger - input
Pin 3  Internal output clock - output
Pin 4  External output clock - input
Pin 5  +5 volts
```

Shunts

Several of the Data Acquisition Processor options are set by shunts. These are jumper wires enclosed in plastic, designed for connecting pins on 0.100" centers.

Each shunt has a top and a bottom. When a shunt is placed correctly, a probe point is visible in the shunt. Shunts must not be placed upside down on the pins, as incorrectly placed shunts do not provide reliable contacts.

Analog Signal Path Selection

In addition to the DAPL configuration options, the Data Acquisition Processor has several hardware configuration options. These determine the path taken by analog signals from the input pins to the analog-to-digital converter.

The analog signal path between the input pins and the analog-to-digital converter consists of the following functional units:

1. input multiplexers
2. instrumentation amplifier
3. programmable gain amplifier
4. unipolar offset circuit
5. analog-to-digital converter with sample and hold amplifier

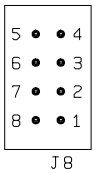
Analog signals must pass through the input multiplexers, the instrumentation amplifier, and the analog-to-digital converter. Jumpers determine whether the analog signal path includes the programmable gain amplifier and the unipolar offset circuit, and also determine the input voltage range.

A signal range is called bipolar if it includes both positive and negative voltages; a signal range is called unipolar if it includes voltages of only one sign. The unipolar offset circuit allows the bipolar analog-to-digital converter to operate with unipolar voltages. Jumpers select from two bipolar ranges and one unipolar range. If the programmable gain amplifier is enabled, gains of 1, 10, 100, and 500 are software selectable.

Analog Signal Path Configuration

The following connectors control the analog signal path of the DAP 1200e and the DAP 2400e. Note that changing voltage ranges may require recalibration.

The input signal to the analog-to-digital converter is selected by J8, a header of two rows on 0.100 inch centers. J8 selects the input voltage range as well as enabling or disabling gain if in bipolar mode. It is often desirable to leave gain enabled, even if only a gain of 1 is used.



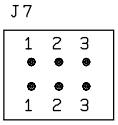
Exactly two jumpers should be placed on J8, as follows:

Jumpers	Signal range
1-8, 3-6	unipolar, 0 to 5 Volts
4-5, 3-6	bipolar, +/- 5 Volts, gain enabled
2-7, 3-6	bipolar, +/- 5 Volts, gain disabled
3-4, 5-6	bipolar, +/- 10 Volts, gain enabled
3-4, 6-7	bipolar, +/- 10 Volts, gain disabled

Note that jumpers on J8 can be placed horizontally or vertically.

Note: Regardless of the input voltage range, positive and negative differential signals may range from -10 volts to +10 volts.

The input signal to the unipolar offset circuit is selected by J7, a header of two rows on 0.100 inch centers.



Exactly one jumper should be placed on J7, as follows:

Jumper	Signal range
1	bipolar
2	unipolar, gain enabled
3	unipolar, gain disabled

The unipolar input range is from 0 to +5 volts.

The following table summarizes the DAP 1200e and the DAP 2400e jumper connections:

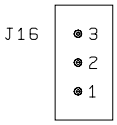
ADC Range	J7	J8
0v to 5v	2	1-8, 3-6
±5v *	1 *	3-6, 4-5 *
±10V	1	3-4, 5-6

* Factory Configuration

Channel List Selection

The Data Acquisition Processor has two possible external input clocking modes. When Channel List Clocking is enabled, all input pins are sampled on each low to high transition of the external clock. When Channel List Clocking is disabled, a single pin is sampled on each low to high transition of the external clock.

Connector J16, located above the left-most gold edge connector, determines the clocking mode for external clocking. J16 is a three pin vertical header of one column on 0.100 inch centers. The factory configuration is “enabled.”

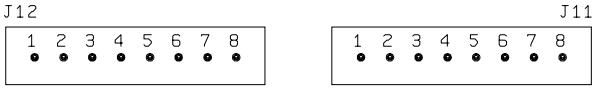


Exactly one jumper should be placed on J16, as follows:

Pins	Channel List Clocking
2,3	disabled
1,2	enabled

Analog Output Voltage Range Selection

The voltage ranges of `DAC0` and `DAC1` are selected by headers `J11` and `J12`, respectively:



Three jumpers should be placed on `J11` and `J12`, as follows:

Jumpers	Range
3 to 4, 5 to 6, 7 to 8	0 volts to +10 volts
1 to 2, 4 to 5, 7 to 8	-5 volts to +5 volts
1 to 2, 4 to 5, 6 to 7	-10 volts to +10 volts

By default, DAPL assumes that the outputs of the digital-to-analog converters are bipolar. If a unipolar output range is selected, the following DAPL command must be issued:

```
OPTION BPOUTPUT=OFF
```

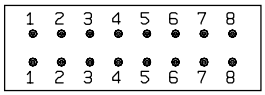
The following table summarizes the DAP 1200e and DAP 2400e output jumper connections:

Voltage Range	J11/DAC0	J12/DAC1
0v to 10v	3-4, 5-6, 7-8	3-4, 5-6, 7-8
±5v *	1-2, 4-5, 7-8 *	1-2, 4-5, 7-8 *
±10V	1-2, 4-5, 6-7	1-2, 4-5, 6-7

* Factory Configuration

Host Configuration Connector

The Host Configuration connector is directly above the gold fingers on the Data Acquisition Processor printed circuit board.



J10 HOST CONFIGURE

Pin pairs 1, 2, and 3 select the I/O address of the Data Acquisition Processor according to the following table:

I/O Address Range	Jumpers
220 - 22F	1,2,3
230 - 23F	2,3
240 - 24F	1,3
250 - 25F	3
320 - 32F	1,2
330 - 33F	2
340 - 34F	1
deselect	none

Pin pairs 4 through 7 select the PC interrupt vector used for communications:

Interrupt Vector	Jumper
2	pin pair 7
3	pin pair 4
4	pin pair 5
5	pin pair 6

A jumper should be connected across exactly one pin pair.

A jumper always should be connected across pin pair 8 for one board in a system. This jumper is provided to allow for several Data Acquisition Processors in one PC. In these systems, exactly one Data Acquisition Processor should have this jumper installed.

Digital Output Reset Polarity Jumper

The digital output reset polarity jumper J32 has two pins spaced at 0.100". J32 is located near the center of the Data Acquisition Processor, approximately 2.5" above J15. The digital output reset polarity jumper allows selection of the digital output polarity at power-on. If J32 is installed, all digital outputs will be reset to 0 at power-on. If J32 is removed, all digital outputs will be preset to 1 at power-on. All Data Acquisition Processors are shipped from the factory with J32 installed. The voltage of the analog outputs at reset may vary by up to 5 millivolts when J32 is removed.

Input/Output Synchronization Header

The input/output synchronization header J22 has two pins spaced at 0.100". J22 is located approximately one inch above the left set of gold fingers on the Data Acquisition Processor. If a shunt is placed on J22, the input trigger is connected to the output update clock. This causes a hardware input trigger to occur when an output procedure initiates its first update. This is used to synchronize input sampling to output updates.

Synchronization Connector

The synchronization connector J13 has a single row of five pins on 0.100 inch centers. J13 is located at the upper left of the Data Acquisition Processor printed circuit board. The synchronization connector allows several Data Acquisition Processors to share the same sampling clock. See Chapter 20 of the Systems Manual for more information about using synchronous Data Acquisition Processors.

For synchronization, the shared sampling clock requires special cabling between Data Acquisition Processors. The analog sampling clock of the master unit is supplied to the slave units by means of the cable MSCBL 015-01. Contact Microstar Laboratories for more information about cabling for synchronous Data Acquisition Processors.

6. DAP 3200e Connectors

This chapter discusses the interface connectors on the DAP 3200e series. Figure 4 and Figure 5 show component placement outlines of the DAP 3200e/x0x and DAP 3200e/x1x. The only components shown are connectors, whose labels begin with the letter J, some integrated circuits, whose labels begin with the letter U, and trim potentiometers, whose labels are single letters.

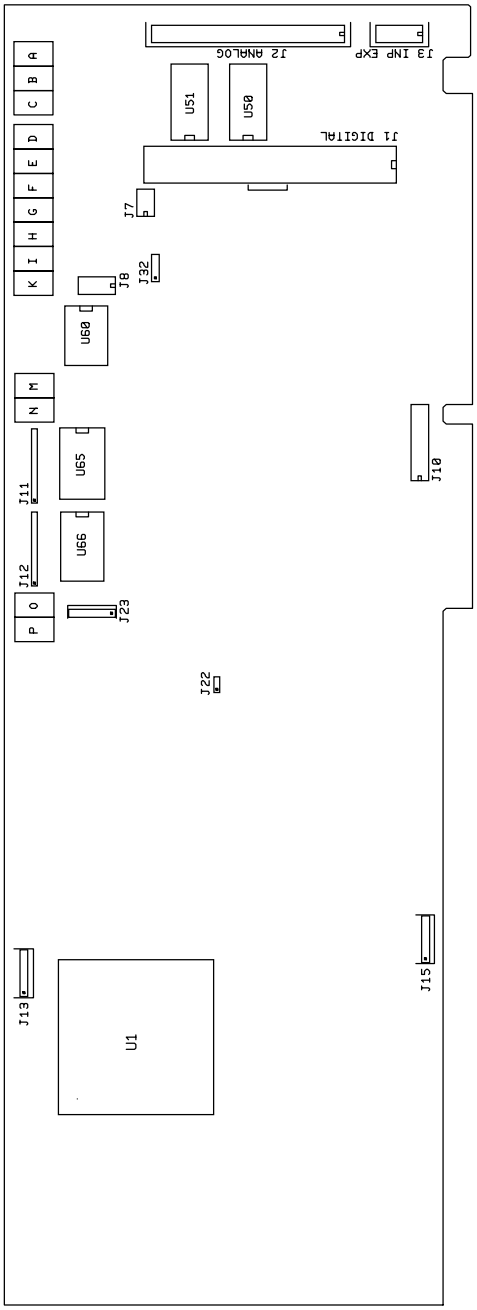


Figure 4.
DAP 3200e/x0x

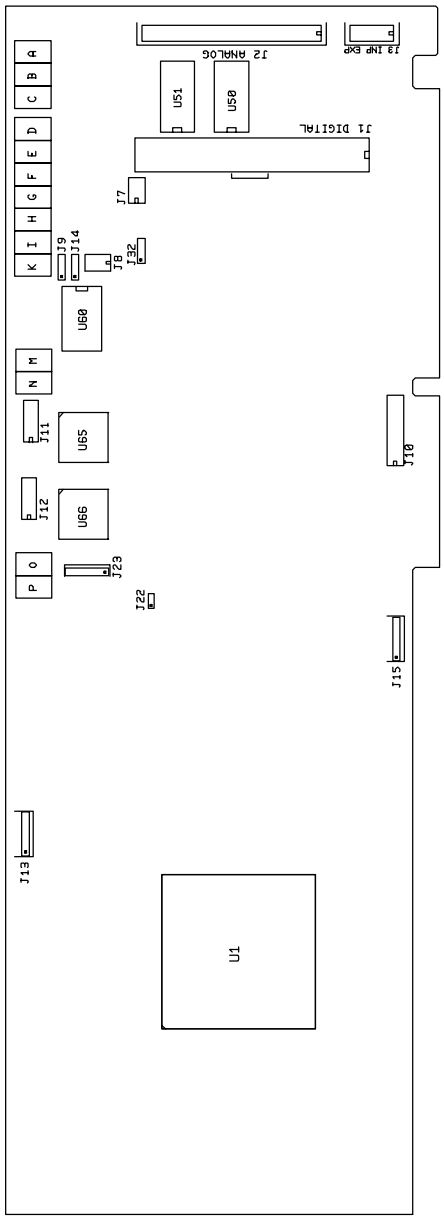


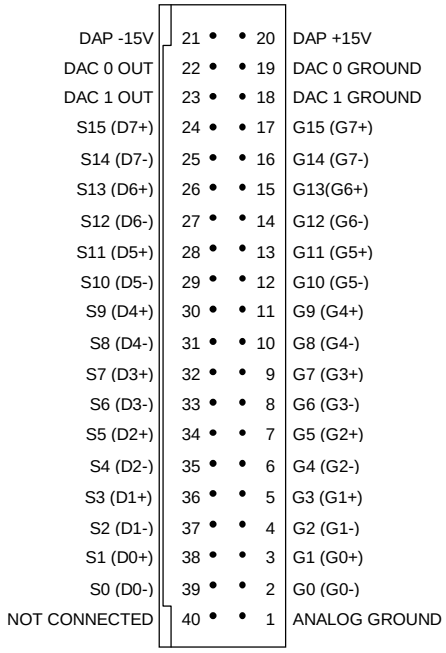
Figure 5.

DAP 3200e/x1x

Analog Input/Output Connector

Analog voltages are connected to the Data Acquisition Processor through a 40 pin analog connector on the back panel of the PC. This connector is located on the right side of the Data Acquisition Processor and is labeled `ANALOG IN/OUT`. It has a double row of pins on 0.100 inch centers. The connector is AMP part number 87476-6. It mates with discrete wire connector AMP 3-87631-6 or insulation displacement connector AMP 499954-8.

Looking at the analog connector from the back of a PC, the pin numbering is:



Note: Use the pin numbering on this chart, rather than numbers which may be found on your connector. Connectors from different manufacturers are not numbered consistently.

Single-ended inputs are indicated by S0 through S15; their corresponding ground inputs are G0 through G15. Differential inputs are indicated by D0- and D0+ through D7- and D7+; their corresponding ground inputs are G0- and G0+ through G7- and G7+. Every differential signal must be referenced to the corresponding ground. Data Acquisition Processors have a limited common mode voltage range and a ground connection must be used to assure that this range is not exceeded.

A single-ended analog signal should be connected to an analog ground pin and to an analog input pin, for example to pins 2 and 39. A differential analog signal should be connected to two adjacent analog input pins and either of their corresponding grounds, for example to input pins 39, 38, and ground pin 2 or 3.

Termination boards to connect all lines of the analog connector to discrete wires are available from Microstar Laboratories.

The DAP 3200e is available either with standard input multiplexers or with fault-protected input multiplexers. Spare fault-protected input multiplexers also are available from Microstar Laboratories.

Analog input signals should be within the range from -10 volts to +10 volts, relative to the ground of the Data Acquisition Processor. With standard input multiplexers, analog input signals should not be applied to the Data Acquisition Processor when the PC's power is off. With fault-protected input multiplexers, input signals may be applied to the Data Acquisition Processor when the PC's power is off. Fault-protected multiplexers protect against voltages up to ±25 volts. Fault-protected multiplexers reduce the maximum sampling speed slightly. See Chapter 7 for electrical characteristics of the analog input pins.

The analog connector of the Data Acquisition Processor includes digital-to-analog converter output pins and analog supply voltages. Pins 22 and 23 are the outputs of DAC0 and DAC1, respectively. Pins 19 and 18 are the grounds for DAC0 and DAC1, respectively. The digital-to-analog converters have voltage outputs with typical output impedance of 0.05 Ohms. These normally should drive high impedance inputs. The output current from each digital-to-analog converter output is rated at ±5 milliamps, but it is recommended that this current not exceed ±1 milliamp.

Analog outputs are set to zero when the system is first powered on. When analog outputs are configured for unipolar mode, the outputs are set to half of the full scale range when the system is first powered on. When J32 is moved, the analog outputs at power-on may vary by up to 5 millivolts.

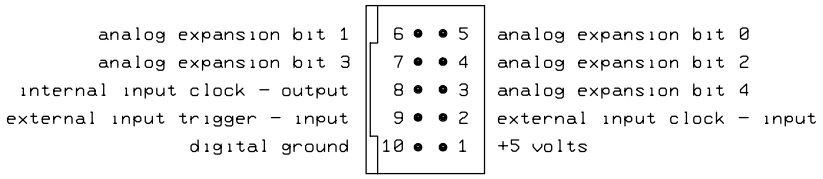
Pin 1 is analog power ground. Pins 20 and 21 are connected to +15 volt and -15 volt analog supplies. The maximum allowable current drain from these supplies is 20 milliamps per side. These supplies can be used for low current, low noise devices such as external multiplexers. To supply power to other devices, either use an external supply or use the 5-volt digital power supply found on the analog control connector with an external DC-to-DC converter.

Analog Control Connector

The analog control connector provides analog input expansion control lines, an external trigger input, an external input clock input, an internal input clock output, and connections to the 5-volt digital supply and its ground. The analog control connector is on the edge of the Data Acquisition Processor, directly below the analog connector. It has two rows of five pins on 0.100 inch centers.

The analog control connector is manufactured by AMP, part number 102570-3. It mates with AMP insulation displacement connector 499499-1 for connection to a ribbon cable or AMP connector 87922-1 for connection to discrete wires.

The DAP 3200e analog control connector, as seen from the back of a PC, has the following pin numbering:



Pins 3 - 7 provide TTL-compatible analog input expansion control signals that select the expansion port. The five highest order bits of the input pin number appear in descending order on pins 3, 7, 4, 6, and 5 for a period starting one sample time before the analog input is sampled.

External analog input expansion boards are available from Microstar Laboratories. Each input expansion board allows up to 32 differential inputs, or up to 64 single-ended inputs, or any combination requiring up to 64 input lines. A Data Acquisition Processor can control up to 8 external expansion boards in parallel, for a total of 512 input lines. See Chapter 13 for more information.

The analog control connector has an input pin for an active high external trigger. Sampling is inhibited if the external trigger is inactive when an input procedure is started. Sampling then commences on the inactive to active transition.

The external trigger is either one-shot or gated, depending on the `HTRIGGER` command in the active input procedure. The external trigger is ignored if there is no `HTRIGGER` command in the active input procedure. See Chapter 8 for more information.

An external trigger signal must be within the standard TTL logic range of 0 to +5 volts. The Data Acquisition Processor provides a pull-up resistor on the external trigger input. This forces the trigger input active if it is left unconnected.

Clock and trigger inputs may have signals applied when the Data Acquisition Processor is off.

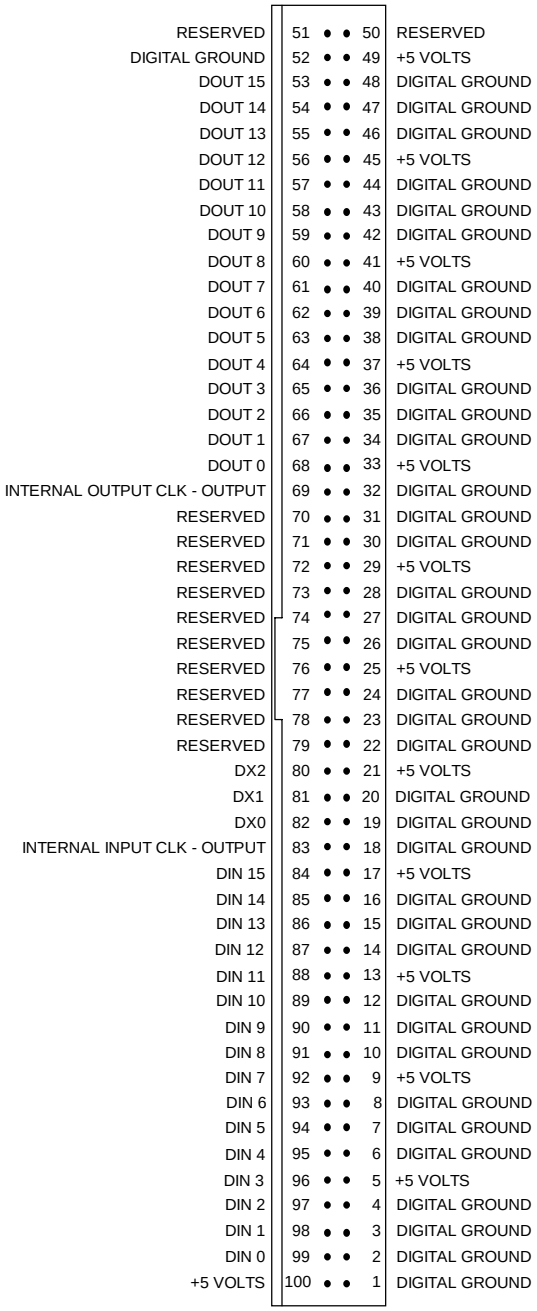
The analog control connector has input and output pins for an external input clock. The input pin should be used to connect an external input clock. The output pin is the buffered output of the internal clock circuit. See Chapter 8 for more information.

Pin 1 provides +5 volt power. Maximum current from this pin is 1 Amp.

Digital Input/Output Connector

The digital input/output connector is a vertical 100-pin connector labeled `J1 DIGITAL`. This connector is near the right edge the Data Acquisition Processor, to the left of the analog input/output connector. Note that this connector is not accessible from the back of the PC. The digital connector has two rows of 50 pins on 0.050 inch centers. The standard connector is manufactured by AMP, part number 1-104549-0. The digital input/output connector mates with insulation displacement connector AMP 1-111196-6.

The pin numbering of the digital input/output connector is shown in the following diagram:


RESERVED 51 50 RESERVED
DIGITAL GROUND 52 49 +5 VOLTS
DOUT 15 53 48 DIGITAL GROUND
DOUT 14 54 47 DIGITAL GROUND
DOUT 13 55 46 DIGITAL GROUND
DOUT 12 56 45 +5 VOLTS
DOUT 11 57 44 DIGITAL GROUND
DOUT 10 58 43 DIGITAL GROUND
DOUT 9 59 42 DIGITAL GROUND
DOUT 8 60 41 +5 VOLTS
DOUT 7 61 40 DIGITAL GROUND
DOUT 6 62 39 DIGITAL GROUND
DOUT 5 63 38 DIGITAL GROUND
DOUT 4 64 37 +5 VOLTS
DOUT 3 65 36 DIGITAL GROUND
DOUT 2 66 35 DIGITAL GROUND
DOUT 1 67 34 DIGITAL GROUND
DOUT 0 68 33 +5 VOLTS
INTERNAL OUTPUT CLK - OUTPUT 69 32 DIGITAL GROUND
RESERVED 70 31 DIGITAL GROUND
RESERVED 71 30 DIGITAL GROUND
RESERVED 72 29 +5 VOLTS
RESERVED 73 28 DIGITAL GROUND
RESERVED 74 27 DIGITAL GROUND
RESERVED 75 26 DIGITAL GROUND
RESERVED 76 25 +5 VOLTS
RESERVED 77 24 DIGITAL GROUND
RESERVED 78 23 DIGITAL GROUND
RESERVED 79 22 DIGITAL GROUND
DX2 80 21 +5 VOLTS
DX1 81 20 DIGITAL GROUND
DX0 82 19 DIGITAL GROUND
INTERNAL INPUT CLK - OUTPUT 83 18 DIGITAL GROUND
DIN 15 84 17 +5 VOLTS
DIN 14 85 16 DIGITAL GROUND
DIN 13 86 15 DIGITAL GROUND
DIN 12 87 14 DIGITAL GROUND
DIN 11 88 13 +5 VOLTS
DIN 10 89 12 DIGITAL GROUND
DIN 9 90 11 DIGITAL GROUND
DIN 8 91 10 DIGITAL GROUND
DIN 7 92 9 +5 VOLTS
DIN 6 93 8 DIGITAL GROUND
DIN 5 94 7 DIGITAL GROUND
DIN 4 95 6 DIGITAL GROUND
DIN 3 96 5 +5 VOLTS
DIN 2 97 4 DIGITAL GROUND
DIN 1 98 3 DIGITAL GROUND
DIN 0 99 2 DIGITAL GROUND
+5 VOLTS 100 1 DIGITAL GROUND

Pins 1 and 100 are closest to the gold edge fingers.

Digital inputs are indicated by `DIN 0-15` and digital outputs are indicated by `DOUT 0-15`. Bit 0 is the least significant bit.

A termination board from Microstar Laboratories, part number MSTB 008-01, connects all lines of the digital connector to discrete wire connectors.

The digital inputs are FCT TTL with 10K pull-up resistors. The digital inputs sink no more than 5 microamps for a “1” input and source no more than 0.5 milliamps for a “0” input. An input voltage greater than 2V is interpreted as a “1” and an input voltage less than 0.8V is interpreted as a “0”. When no signal is connected a digital input is read as a “1” due to the pull-up resistors.

Digital inputs may have TTL signals applied when the Data Acquisition Processor is off.

Digital output polarity at power-on is selected by `J32`, the Digital Output Reset Polarity Jumper, described later in this chapter.

The digital outputs are ACT TTL; they can sink no more than 24 milliamps for a “0” output and can source no more than 24 milliamps for a “1” output. The output voltage for a “1” is greater than 3.8V and the output voltage for a “0” is less than 0.44V.

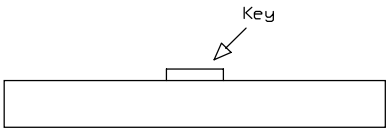
The digital input/output connector has multiple connections to the Data Acquisition Processor +5V power supply. The supply current is rated at 500 milliamps per connection with a total current limit of 2 Amps. The 2 Amp current limit is due to the limited current available from the host computer.

Pins 80, 81, and 82 provide TTL-compatible digital input expansion control signals. The low-order bit of the port number appears on pin 82, the middle bit appears on pin 81, and the high-order bit appears on pin 80.

An optional digital input port may be specified in a DAPL `SET` command. The digital input port numbers range from 0 to 7. The specified port number appears on the control pins for a period starting one sample time before the time at which the digital inputs are sampled. The port number can be used to control external multiplexers.

An external digital expansion board is available from Microstar Laboratories. Each external expansion board allows up to 64 digital inputs and 64 digital outputs.

The Microstar Laboratories cable MSCBL 036-01 is compatible with the digital input/output port. The diagram below shows the key on the cable MSCBL 036-01. This key must be towards the left side of the Data Acquisition Processor.



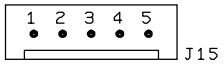
Note: Cables not made by Microstar Laboratories may have different keys.

Output Clock Connector

Connector `J15` is a five pin connector, Molex part number 22-23-2051; the mating connector is Molex part number 22-01-3057. `J15` is located on the lower edge of the Data Acquisition Processor, towards the left side of the board.

The output clock signals and the output trigger signal are on connector `J15`, along with power and ground.

The pin numbering for `J15` is given in the following table:



Pin 1 Ground
Pin 2 External output trigger – input
Pin 3 Internal output clock – output
Pin 4 External output clock – input
Pin 5 +5 volts

Shunts

Several of the Data Acquisition Processor options are set by shunts. These are jumper wires enclosed in plastic, designed for connecting pins on 0.100" centers.

Each shunt has a top and a bottom. When a shunt is placed correctly, a probe point is visible in the shunt. Shunts must not be placed upside down on the pins, as incorrectly placed shunts do not provide reliable contacts.

Analog Signal Path Selection

In addition to the DAPL configuration options, the Data Acquisition Processor has several hardware configuration options. These determine the path taken by analog signals from the input pins to the analog-to-digital converter.

The analog signal path between the input pins and the analog-to-digital converter consists of the following functional units:

1. input multiplexers
2. instrumentation amplifier
3. programmable gain amplifier
4. range amplifier
5. analog-to-digital converter with sample and hold amplifier

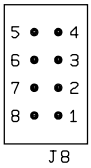
Analog signals must pass through the input multiplexers, the instrumentation amplifier, and the analog-to-digital converter. Jumpers determine whether the analog signal path includes the programmable gain amplifier and the range amplifier, and also determine the input voltage range.

A signal range is called bipolar if it includes both positive and negative voltages; a signal range is called unipolar if it includes voltages of only one sign. The range amplifier allows the bipolar analog-to-digital converter to operate with unipolar voltages. Jumpers select from two bipolar ranges and one unipolar range. If the programmable gain amplifier is enabled, gains of 1, 10, 100, and 500 are software selectable.

Analog Signal Path Configuration, DAP 3200e/x0x

The following connectors control the analog signal path of the DAP 3200e/x0x. Note that changing voltage ranges may require recalibration.

The input signal to the analog-to-digital converter is selected by J8, a header of two rows on 0.100 inch centers. J8 selects the input voltage range as well as enabling or disabling gain if in bipolar mode. It is often desirable to leave gain enabled, even if only a gain of 1 is used.



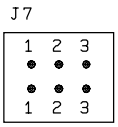
Exactly two jumpers should be placed on J8, as follows:

Jumpers	Signal range
1-8, 3-6	unipolar, 0 to 5 Volts
4-5, 3-6	bipolar, +/- 5 Volts, gain enabled
2-7, 3-6	bipolar, +/- 5 Volts, gain disabled
3-4, 5-6	bipolar, +/- 10 Volts, gain enabled
3-4, 6-7	bipolar, +/- 10 Volts, gain disabled

Note that jumpers on J8 can be placed horizontally or vertically.

Note: Regardless of the input voltage range, positive and negative differential signals may range from -10 volts to +10 volts without damaging the Data Acquisition Processor.

The input signal to the unipolar offset circuit is selected by J7, a header of two rows on 0.100 inch centers.



Exactly one jumper should be placed on J7, as follows:

Jumper	Signal Range
1	bipolar
2	unipolar, gain enabled
3	unipolar, gain disabled

The unipolar input range is from 0 to +5 volts.

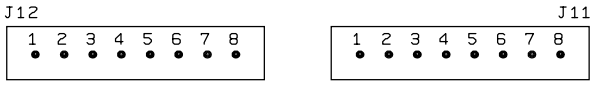
The following table summarizes the DAP 3200e/x0x jumper connections:

ADC Range	J7	J8
0v to 5v	2	1-8, 3-6
±5v	1 *	3-6, 4-5 *
±10v	1	3-4, 5-6

*Factory Configuration

Analog Output Voltage Range Selection, DAP 3200e/x0x

The voltage ranges of DAC0 and DAC1 are selected by headers J11 and J12, respectively:



Three jumpers should be placed on J11 and J12, as follows:

Jumpers	Range
3 to 4, 5 to 6, 7 to 8	0 volts to +10 volts
1 to 2, 4 to 5, 7 to 8	-5 volts to +5 volts
1 to 2, 4 to 5, 6 to 7	-10 volts to +10 volts

By default, DAPL assumes that the outputs of the digital-to-analog converters are bipolar. If a unipolar output range is selected, the following DAPL command must be issued:

```
OPTION BPOUTPUT=OFF
```

The following table summarizes the DAP 3200e/x0x output jumper connections:

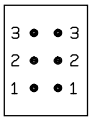
Voltage Range	J11/DAC0	J12/DAC1
0v to 10v	3-4, 5-6, 7-8	3-4, 5-6, 7-8
±5v	1-2, 4-5, 7-8 *	1-2, 4-5, 7-8 *
±10v	1-2, 4-5, 6-7	1-2, 4-5, 6-7

*Factory Configuration

Analog Signal Path Configuration, DAP 3200e/x1x

The following connectors control the analog signal path of the DAP 3200e/x1x. Note that changing voltage ranges may require recalibration.

The input signal to the analog-to-digital converter is selected by `J8`, a header of two rows on 0.100 inch centers.



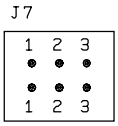
J8

Exactly one jumper should be placed on `J8`, as follows:

Jumper	Analog-to-digital converter input
1	instrumentation amplifier
2	programmable gain amplifier
3	range amplifier

Note that jumpers on `J8` are placed horizontally.

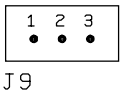
The input signal to the range amplifier is selected by J7, a header of two rows on 0.100 inch centers.



Exactly one jumper should be placed on J7, as follows:

Jumper	Range amplifier input
1	range amplifier disabled
2	programmable gain amplifier
3	instrumentation amplifier

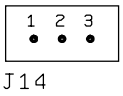
The signal range of the range amplifier is selected by J9 and J14. J9 selects between unipolar inputs and bipolar inputs.



One jumper should be placed on J9 as follows:

Jumper	Signal range
1-2	unipolar
2-3	bipolar

J14 selects the input signal range of the range amplifier.



One jumper should be placed on J14 as follows:

Jumper	Input signal range
1-2	0 to 5 Volts
1-2	± 2.5 Volts
1-2	± 5 Volts
2-3	± 10 Volts

Note: Regardless of the input voltage range, positive and negative differential signals may range from -10 volts to +10 volts without damaging the Data Acquisition Processor.

Note: There is a maximum speed reduction for the +/- 10-volt input range on the DAP 3200e/x1x. Using the input voltage of +/- 10 volts, the minimum `TIME` is 2.4 us, which is approximately 417 Ksamples/second.

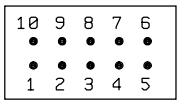
The following table summarizes the DAP 3200e/x1x jumper connections:

ADC Range	J7	J8	J9	J14
0 to 5 v	2	3	1 - 2	1 - 2
± 2.5v	1	2	2 - 3	1 - 2
± 5v	2	3	2 - 3 *	1 - 2 *
± 10 v	2	3	2 - 3	2 - 3

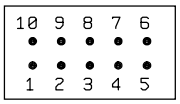
* Factory Configuration

Analog Output Voltage Range Selection, DAP 3200e/x1x

The voltage ranges of `DAC0` and `DAC1` are selected by headers `J11` and `J12`, respectively:



J12



J11

Three or four jumpers should be placed on `J11` and `J12`, as follows:

Jumpers	Range
2-3, 8-9, 4-5, 6-7	0 to 5 Volts
2-3, 8-9, 6-7	0 to 10 Volts
1-2, 9-10, 4-5, 6-7	± 2.5 Volts
1-2, 9-10, 6-7	± 5 Volts
1-2, 9-10, 5-6	± 10 Volts

By default, DAPL assumes that the outputs of the digital-to-analog converters are bipolar. If a unipolar output range is selected, the following DAPL command must be issued:

```
OPTION BPOUTPUT=OFF
```

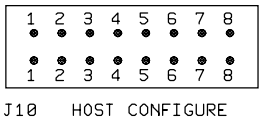
The following table summarizes the DAP 3200e/x1x output jumper connections:

Voltage Range	J11/DAC0	J12/DAC1
0 to 5v	2-3, 8-9, 4-5, 6-7	2-3, 8-9, 4-5, 6-7
0 to 10v	2-3, 8-9, 6-7	2-3, 8-9, 6-7
± 2.5v	1-2, 9-10, 4-5, 6-7	1-2, 9-10, 4-5, 6-7
± 5v *	1-2, 9-10, 6-7 *	1-2, 9-10, 6-7 *
± 10 v	1-2, 9-10, 5-6	1-2, 9-10, 5-6

* Factory Configuration

Host Configuration Connector

The Host Configuration connector is directly above the gold fingers on the Data Acquisition Processor printed circuit board.



J10 HOST CONFIGURE

Pin pairs 1, 2, and 3 select the I/O address of the Data Acquisition Processor according to the following table:

I/O Address Range	Jumpers
220 - 22F	1,2,3
230 - 23F	2,3
240 - 24F	1,3
250 - 25F	3
320 - 32F	1,2
330 - 33F	2
340 - 34F	1
deselect	none

Pin pairs 4 through 7 select the PC interrupt vector used for communications:

Interrupt Vector	Jumper
2	pin pair 7
3	pin pair 4
4	pin pair 5
5	pin pair 6

A jumper should be connected across exactly one pin pair.

A jumper always should be connected across pin pair 8 for one board in a system. This jumper is provided to allow for several Data Acquisition Processors in one PC. In these systems, exactly one Data Acquisition Processor should have this jumper installed.

Digital Output Reset Polarity Jumper

The digital output reset polarity jumper J32 has three pins spaced at 0.100". J32 is located in the upper right section of the Data Acquisition Processor, directly below J8. The digital output reset polarity jumper allows selection of the digital output polarity at power-on. If J32 is installed on pins 1-2 (pin 1 is on the left), all digital outputs will be reset to 0 at power-on. If J32 is installed on pins 2-3, all digital outputs will be preset to 1 at power-on. All Data Acquisition Processors are shipped from the factory with J32 installed on pins 1-2. The voltage of the analog outputs at reset may vary by up to 5 millivolts when J32 is moved.

Input/Output Synchronization Header

The input/output synchronization header J22 has two pins spaced at 0.100". J22 is located approximately two inches above the left set of gold fingers on the Data Acquisition Processor. If a shunt is placed on J22, the input trigger is connected to the output update clock. This causes a hardware input trigger to occur when an output procedure initiates its first update. This is used to synchronize input sampling to output updates.

Synchronization Connector

The synchronization connector J13 has a single row of five pins on 0.100 inch centers. J13 is located at the upper left of the Data Acquisition Processor printed circuit board. The synchronization connector allows several Data Acquisition Processors to share the same sampling clock. See the Systems Manual for more information about using synchronous Data Acquisition Processors.

For synchronization, the shared sampling clock requires special cabling between Data Acquisition Processors. The analog sampling clock of the master unit is supplied to the slave units by means of the cable MSCBL 015-01. Contact Microstar Laboratories for more information about cabling for synchronous Data Acquisition Processors.

Cooling Space Requirement

The DAP 3200e/415, DAP 3200e/315 and DAP 3200e/214 use clock-doubled processors that require heat sinks for cooling. The DAP 3200e/315 uses a tall heat sink that takes up the space of two expansion slots. Consequently, an expansion card can not be installed in the slot adjacent to the DAP 3200e/315 in the computer. The additional space is required in systems with low air flow around the Data Acquisition Processor. For systems with sufficient air flow, an optional short heat sink is available from Microstar Laboratories that allows an expansion card to be installed in the adjacent slot. With an expansion card installed in the adjacent slot, the user must make sure there is an air flow of at least 400 linear feet per minute over the heat sink in order to guarantee adequate cooling.

Caution: Failure to meet this requirement can damage the Data Acquisition Processor.

The DAP 3200e/415 and DAP 3200e/214 use short heat sinks that allow an expansion card to be installed in the adjacent slot.

7. Analog Input Circuits

The analog input hardware of the Data Acquisition Processor is discussed in some detail in this chapter. The following summary gives sufficient information for most Data Acquisition Processor applications:

- he DC input impedance is very high.
- at high sampling rates, the signal source impedance should be low.
- minimum sampling times are specified for unity gain.
- at gain 10, the fastest sampling rate is slower than the fastest sampling rate at gain 1.
- at gain 100, 500, and 1,000, the fastest sampling rate is substantially slower than the fastest sampling rate at gain 1.
- fault-protected multiplexers typically increase the minimum sampling time by 2 µs at gain 1 and at gain 10, and by 5 µs at gain 100, 500, and 1,000.

Analog Input Circuits

Data Acquisition Processors through two analog multiplexers and then to an op amp with a FET input. The DC input impedance is very high, typically far in excess of 10M Ohms. The AC input impedance is dominated by the capacitance of the multiplexers.

Figure 6 shows a useful equivalent circuit for each Data Acquisition Processor input. As the Data Acquisition Processor scans through the input pins defined by an input procedure, the switches in the multiplexers open and close, connecting the specified inputs to multiplexer outputs. When an input signal is connected to the FET amplifier, the signal source must supply sufficient current to charge the equivalent capacitance of the multiplexers before the analog-to-digital conversion can start.

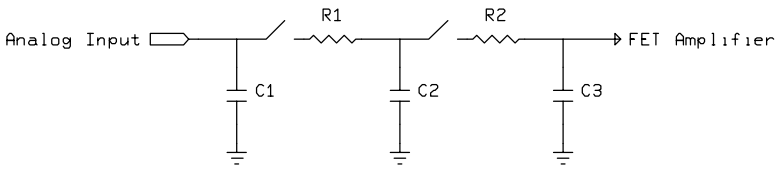


Figure 6.

Data Acquisition Processors are available either with standard multiplexers or with fault-protected multiplexers. The following table shows typical resistance and capacitance values, in Ohms and picofarads, for Data Acquisition Processors with standard multiplexers and with fault-protected multiplexers.

	Standard	Fault-Protected
R1	40	1500
R2	40	40
C1	11	5
C2	65	36
C3	39	39

The higher series resistance of the fault-protected multiplexers increases the minimum sampling time. This effect must be considered with all Data Acquisition Processor models except for the DAP 800. On other models, the minimum sampling time is increased by approximately 2 microseconds at gains of 1 and 10, and by approximately 5 microseconds at gains of 100, 500, and 1,000.

Programmable Gain Amplifier

At gains other than unity, the programmable gain amplifier requires extra time to switch from pin to pin and then settle to full accuracy. The following table shows typical minimum sampling times for each Data Acquisition Processor at each gain.

Model	Minimum Sample Time in uS at Gain				
	1	10	100	500	1000
800/1	13.20	13.2	40	-	500
800/2 and /3	9.50	9.5	40	-	500
801/1	13.20	13.2	40	-	500
1200e/4	6.00	8	40	500	-
1200e/6	3.20	8	40	500	-
2400e/4	6.00	8	40	500	-
2400e/5	4.00	8	40	500	-
2400e/6	3.20	8	40	500	-
3200e/x0x	3.00	8	40	500	-
3200e/x1x	1.30	8	40	500	-

8. Clocks and Triggers

The Data Acquisition Processor is designed to operate either using internal clocks or using external clocks. The Data Acquisition Processor has on-board crystal controlled timers to provide an internal input sampling rate and output update rate, and also has provisions for external clocks for both input and output.

The Data Acquisition Processor has hardware control lines for an input clock, an output clock, and an input trigger. The e Series Data Acquisition Processors also have a hardware control line for an output trigger. These lines all are TTL compatible. The input clock and the output clock both are positive edge triggered.

The input clock on all models has two modes. In the first mode, the Data Acquisition Processor starts conversion of an entire channel list on the positive edge of the clock. In the second mode, the Data Acquisition Processor converts a single channel on the positive edge of the clock. The first mode is called Channel List Clocking. The output clock of the DAP 3200e also has these modes.

The input trigger and output trigger on all models also have two modes, a one-shot mode and a level triggered gate mode.

Software Triggers vs. Hardware Triggers for Input

DAPL provides a powerful software triggering mechanism which is suitable for most applications. For those applications which require precise synchronization to external hardware or which are too fast to take advantage of software triggering, hardware triggering is provided. Software triggering is more versatile than hardware triggering. In applications with sampling rates of less than 10 KHz, software triggering almost always provides a better solution than hardware triggering.

Software triggers rely on DAPL tasks to scan input data to detect events within the data. When an event is detected, a task asserts a software trigger. After the trigger is asserted, another task may act, based on the assertion. The most common action is to pass a number of values around the trigger event either to another task or to the PC. The trigger mechanism is much like the trigger on an oscilloscope. Since all of the processing functions of DAPL may be used to define events, however, much more complex events may be detected.

Hardware input triggers are implemented using a digital control line which is separate from the sampling stream. This control line starts and stops input sampling. Since the trigger line is not dependent on the input data, external hardware must be provided to detect events of interest.

Software triggers have several advantages over hardware triggers. First, a software trigger may be changed by changing a few lines in a DAPL command list. In contrast, a hardware trigger event must be detected by external hardware which may be inflexible and costly to modify. Second, software triggers scan input data to detect events, so pretrigger data are available. Because a hardware trigger starts the Data Acquisition Processor input section, no samples are taken before a trigger event. Finally, with software triggers DAPL provides precise timing information. With hardware triggers DAPL is not able to provide accurate timing information because hardware triggers start and stop input sampling at undefined times.

Hardware triggering does provide precise synchronization of acquisition to external events. Hardware triggering also allows detection of events which are too fast to process with software triggers.

Software and hardware triggering are implemented separately and may be used together.

External Input Clock

The external input clock is a positive-edge triggered TTL signal. The external input clock is activated by the command `CLOCK EXTERNAL` in an input procedure. The `TIME` command of an input procedure with input clocking enabled must be at least tSYNCH less than the period of the external clock. tSYNCH is defined at the end of this chapter.

External input clocking has two modes. The first mode, called Channel List Clocking, starts conversion of an entire channel list on the positive edge of the external clock. The second mode converts a single channel on the positive edge of the external clock. On the DAP 3200e, the selection between the modes is made by a parameter to the `CLCLOCKING` command in an input procedure. The two options for `CLCLOCKING` are `ON` and `OFF`. The default is `ON`. On the DAP 800, DAP 1200e, and DAP 2400e, the selection between the modes is made by the position of a shunt on connector `J16`. As the Data Acquisition Processor is shipped from Microstar Laboratories, Channel List Clocking is selected. See Chapter 4 or 5 for a diagram of `J16`.

Example:

```
IDEF A 5
   CLOCK EXTERNAL
   SET IPIPE0 S0
   SET IPIPE1 S1
   SET IPIPE2 S2
   SET IPIPE3 S3
   SET IPIPE4 S4
   TIME 1000
. . . .
   END
```

Example (DAP 3200e only):

```
IDEF A 5
    CLOCK EXTERNAL
    CLCLOCKING ON
    SET IPIPE0 S0
    SET IPIPE1 S1
    SET IPIPE2 S2
    SET IPIPE3 S3
    SET IPIPE4 S4
    TIME 1000
. . . .
    END
```

In this application, external input clocking is enabled for the input procedure `A`. With Channel List Clocking selected, each positive edge of the external clock causes conversion of the entire channel list consisting of channel 0 (`S0`) to channel 4 (`S4`). The channels are converted in sequence with channel 0 synchronized to the positive edge of the external clock and each of the subsequent channels converted according to the `TIME` command. Channel 1 (`S1`) is converted 1000 µs following the edge of the external clock, channel 2 (`S2`) is converted 2000 µs following the edge of the external clock, up to channel 4 (`S4`) which is converted 4000 µs following the edge of the external clock. When using Channel List Clocking, the period of the external clock (rising edge to rising edge) must be greater than the `TIME` command times the number of channels plus tSYNCH. The external clock may be as slow as required—there is no maximum period.

In the previous application, the external clock must have a minimum period of 5000 µs plus tSYNCH. For example, on a DAP 2400e/4, the time for tSYNCH is 0.25 µs, so the minimum period of the external clock is 5000.25 µs. The value of 0.25 µs is calculated as 4/16, where 16 is the CPU clock speed in MHz.

If single channel clocking is selected rather than Channel List Clocking, each positive edge of the external clock causes conversion of only one channel. The channels are converted in sequence. Each channel is synchronized to a positive edge of the external clock. In the previous application, channel 0 (`S0`) is converted on the first edge of the external clock, channel 1 (`S1`) is converted on the second edge of the external clock, and so on up to channel 4 (`S4`), which is converted on the fifth edge of the external clock. The channel list then is repeated with channel 0 converted again on the sixth positive edge of the external clock. When using single channel clocking, the period of the external clock (rising edge to rising edge) must be greater than the `TIME` command plus tSYNCH. The external clock may be as slow as required; there is no maximum period.

In the previous application, the external clock must have a period of 1000 µs plus tSYNCH. For example, on a DAP 2400e/4, the time for tSYNCH is 0.25 µs, so the minimum period of the external clock is 1000.25 µs.

Early External Input Clock Edges

For the DAP 800, DAP 1200e, and DAP 2400e, to guarantee that acquisition only occurs on external clock edges requires that there are no extra external input clock edges between 200 ns and tSYNCH plus the `TIME` command after the last acquisition. If this is not prevented, the Data Acquisition Processor will continue to operate, but the next acquisition will start according to the `TIME` command, not the external clock. Clocks earlier than 200 ns from the last acquisition are ignored.

In the previous example with channel list clocking, the external clock must not rise between 4000 µs plus 200 ns (4000.2 µs) and 5000 µs plus tSYNCH after the external clock that channel 0 converted upon. Extra clock edges less than 4000.2 µs after the clock for channel 0 are guaranteed to be ignored. Edges after that time and before 5000 µs plus tSYNCH can cause the next channel list to start 1000 µs after channel 4 (`S4`), instead of at the time of an external clock.

In the previous example with single channel clocking, the external clock should not rise between 200 ns and 1000 µs plus tSYNCH after any external clock that causes an acquisition. Any clock edge that does not meet this requirement will cause the next channel to be converted 1000 µs after the previous channel, instead of being converted upon an external clock edge.

The DAP 2400e does not have this requirement. Any external clock edges appearing before the `TIME` command plus tSYNCH are ignored.

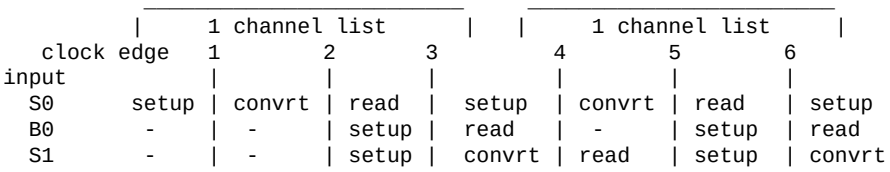
Input Pipeline Timing

This section is of interest only when using external clocking or low latency with internal clocking. For DAP 3200e hardware timing, see the next section.

Input sampling hardware has one pipeline stage for digital inputs and two pipeline stages for analog inputs. The number of pipeline stages and the type of the first input channel determines the number of clock pulses that are needed for the CPU to read a given value.

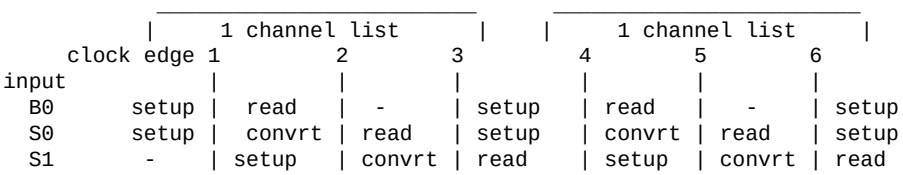
If the first channel is analog, analog conversion occurs on the first clock pulse and the value is read by the CPU on the second clock pulse. For channel list clocking, the last value in the channel list is read on the next external clock edge. The following timing

diagram shows the relation of analog and digital samples when the first channel is analog. Note that for external clocking, one additional clock pulse is required before the first clock pulse shown in this diagram. See the Input clocking startup considerations section later in this chapter for more details.



Note that `setup` indicates the setup of analog or digital input circuits, `convrt` indicates when the value is held and converted to digital, and `read` indicates when the value is read by the CPU. Each action occurs at or soon after the previous clock edge in the diagram.

If the first channel is a binary input and channel list clocking is used, the next clock pulse is not required to read the value from the last channel in the list. If one or more binary channels are used in a channel list with external clocking, it is best to make the first channel binary to simplify the timing. The following timing diagram shows relative timing when the first channel is binary.



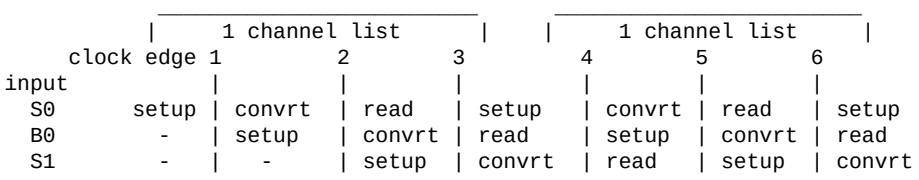
The pipeline is important to consider in low latency applications. The time between the beginning of conversion and when the value is read by the CPU adds to the total response latency of the Data Acquisition Processor. For analog inputs one sample period is added to the latency. No significant latency is added for digital inputs.

DAP 3200e Input Pipeline Timing

This section is only of interest when using external clocking or low latency with internal clocking.

The DAP 3200e has two pipeline stages for analog and digital inputs. The timing is the same for both. An acquired value is read by the CPU after the following clock edge. This causes one sample period of time to be added to Data Acquisition Processor response latency. When channel list clocking is used with an external clock, the last value of the channel list is not read until the following external clock. There are several cases described later that increase the number of extra clocks that are necessary before the expected number of values are read.

The following timing diagram illustrates the input timing for the DAP 3200e.



Note that `setup` indicates the setup of analog or digital input circuits before the value is sampled, `convrt` indicates when the value is held and converted to digital, and `read` indicates the value is read by the CPU. Each action occurs at or soon after the previous clock edge in the diagram.

The DAP 3200e analog pipeline increases when analog and digital are used together to achieve aggregate input speeds higher than the maximum analog input rate. The digital input pipeline remains unchanged. The analog input pipeline increases to allow enough time for the analog-to-digital conversion.

When arranging the channel list, the time between analog input samples must be equal to or greater than the minimum analog input sample time. Digital inputs can be placed between analog inputs to give the analog inputs enough time to convert. The number of clock cycles for analog conversion can be calculated by the following formula:

```
Cycles = roundup (Minimum Time / TIME)
```

`Minimum Time` is the minimum analog sample time for the DAP 3200e. `TIME` is the sample time used in the input procedure.

Normally one extra clock pulse is required before DAPL can read each value. In special cases, the extra cycles cause garbage values to be read and ignored at the beginning of sampling or at the beginning of each burst. The garbage values are significant when using external clocking because they each require an extra clock pulse before the expected number of values are read by DAPL.

When high-speed sampling is used, the number of extra clock pulses after the first clock can be calculated by the following rules:

- If all channels are binary, one extra clock is required. This is the same as for normal-speed sampling.
- Otherwise, there are `Cycles - B` extra required clocks. Cycles is calculated above and B is the number of binary channels before the first analog channel. There always is at least one extra clock required before the expected number of values is read by DAPL. It is best to put binary channels first in the channel list to reduce the number of extra clocks required.

The following timing diagram example for the DAP 3200e shows how the analog input pipeline is increased when analog and digital inputs are combined for an aggregate rate of 1 MHz. Note that for a `TIME` of 1.0 there are four clock cycles required for the analog input pipeline.

```
          _____________________________      _____________________________
         |    1 channel list      |     |     1 channel list     |
     clock edge 1         2        3         4        5        6
input           |         |        |         |        |        |
  S0      setup | convrt                      | read
                | setup                       | convrt
  B0      setup | convrt  | read*  | setup    | convrt | read   | setup
  B1       -    | setup   | convrt | read*    | setup  | convrt | read
```

Note that the analog circuits setup for the next conversion while the current sample is being converted to digital. * indicates the value read is a garbage value. These values are thrown away by DAPL to ensure the correct order of values in input channel pipes.

External Output Clock

For most applications, there is no need to provide an output clock source to the Data Acquisition Processor; the on-board timer provides a wide range of update frequencies with fine time resolution. The main use of an output clock is to precisely match the output update rate to a standard frequency.

The external output clock on the Data Acquisition Processor is a positive edge triggered TTL signal. Similar to the external input clock, the output clock is activated by the command `CLOCK EXTERNAL` in an output procedure. The `TIME` command of an output procedure with output clocking enabled must be at least tSYNCH shorter than the external clock period. tSYNCH is defined at the end of this chapter. Unlike the external input clock, the first external output clock pulse is recognized.

On the DAP 3200e, external output clocking has two modes. The first mode, called Channel List Clocking, starts output of an entire channel list on the positive edge of the external clock. The second mode outputs a single channel on the positive edge of the external clock. The selection between the modes is made by a parameter to the `CLCLOCKING` command in an output procedure. The two options for `CLCLOCKING` are `ON` and `OFF`. The default is `ON`.

On the DAP 800, DAP 1200e, and DAP 2400e, all channels are updated simultaneously on the external clock.

Hardware Input Trigger

There are two modes for the input trigger. The first is a one-shot mode and the second is a level controlled gated mode. The mode of the hardware trigger is selected by a parameter to the `HTRIGGER` command in an input procedure. The three options for `HTRIGGER` are `ONESHOT`, `GATED`, and `OFF`. The default is `OFF`.

In the one-shot mode, the trigger line is held in a low state when an input procedure is started. Input sampling does not start until the trigger line is high. Sampling continues until a `STOP` command is issued or the number of samples specified by the `COUNT` command of the input procedure is reached. The first sampled value is precisely synchronized to the trigger edge and all subsequent values are within ± tSYNCH of the `TIME` command of the input procedure. tSYNCH is defined at the end of this chapter. The active period of the external input trigger must be greater than 60 ns to guarantee proper operation.

In the level-triggered gated mode, input sampling may start and stop repeatedly, depending on the level of the trigger signal. The input is sampled continuously when the trigger signal is high. Input sampling stops when the trigger signal is low.

When input clocking is configured in Channel List Clocking mode, the input is stopped only at channel list boundaries. When input clocking is configured to clock single channels, the input is stopped on channel boundaries. The effect of this is that the start of sampling is precisely synchronized to the positive edge of the trigger signal, assuming that sampling has stopped. Sampling stops when the Data Acquisition Processor has completed sampling of either a channel list or a channel. When input sampling has been stopped with the gated trigger, synchronization of sampling to the positive edge of the trigger signal is the same as for the one-shot mode.

e-Series Hardware Output Trigger

There are two modes for the output trigger of e Series Data Acquisition Processor. The first mode is a one-shot mode and the second mode is a level-controlled gated mode. The mode of the hardware trigger is selected by a parameter to the `HTRIGGER` command in an output procedure. The three options for `HTRIGGER` are `ONESHOT`, `GATED`, and `OFF`. The default is `OFF`.

In the one-shot mode, the trigger line is held in a low state when an output procedure is started. Output updating does not start until the trigger line is high. Updating continues until a `STOP` command is issued or the number of updates specified by the `COUNT` command of the output procedure is reached. The first updated value is precisely synchronized to the trigger edge and all subsequent values are within +/- tSYNCH of the `TIME` command of the output procedure. tSYNCH is defined at the end of this chapter. The active period of the external output trigger must be greater than 60 ns to guarantee proper operation.

In the level-triggered gated mode, output updating may start and stop repeatedly, depending on the level of the trigger signal. The output is updated continuously when the trigger signal is high. Output updating stops when the trigger signal is low. The active period of the output trigger must be less than the sampling time of the output procedure minus 50 ns to guarantee that only one update occurs.

On the DAP 3200e, when output clocking is configured in Channel List Clocking mode, the output is stopped only at channel list boundaries. When output clocking is configured to clock single channels, the output may stop after any channel. The effect of this is that the start of output is precisely synchronized to the positive edge of the trigger signal, assuming that output has stopped. Output stops when the Data Acquisition Processor has completed output of either a channel list or a channel. When output has been stopped with the gated trigger, synchronization of output to the positive edge of the trigger signal is the same as for the one-shot mode.

On the DAP 800, DAP 1200e, and DAP 2400e, all channels are updated simultaneously on the external clock.

Timing Considerations

When an external clock is used, the time of an event with respect to the start of sampling may only be determined if the period of the external clock is known. DAPL establishes event times as sample times. If the external clock period is variable or the period is unknown, the time of an event cannot be determined. The event's sample number may still be useful in other contexts. Note that the results of all frequency domain processing such as `FREQUENCY`, `FFT`, and `RFILTER` depend on the period of the external clock and may not be defined if the external clock period varies.

When hardware triggering is used, DAPL provides timing information relative to the start of each external trigger. In a case of a one-shot trigger, sampling or output updating starts on a single event so all timing information is relative to the trigger event. In the case of a gated trigger, sampling or output updating may start or stop at arbitrary times. Timing information may still be obtained if means are provided to distinguish one external trigger event from the next.

Input Clocking Startup Considerations

For the DAP 800, DAP 1200e, and DAP 2400e, following the start of an input procedure with external input clocking enabled, there is a delay of one external clock edge before the first input sample is taken. This delay is required to allow clean synchronization of the internal clock to the external input clock. This means that the first positive edge of the external input clock, following the `START` command to the input procedure, is ignored. The second positive edge of the external input clock may be as close as 50 ns to the first positive edge.

If loss of the first external clock edge is unacceptable, the input trigger, configured in the level triggered gated mode, may be used as an input clock. This requires the input trigger to have a short active period. The active period of the input trigger should be more than 60 ns; this allows for any speed of acquisition. The active period of the input trigger must be 200 ns or less to guarantee that only one acquisition occurs.

If the input trigger is held inactive until the input procedure is started, the first positive edge of the input trigger will cause a conversion. Note that this approach to clocking seldom makes sense when the external clock source is free running; in most cases, using external hardware to provide a clean trigger signal will lose one clock edge.

The DAP 3200e does not have a delay of one external clock edge. The first input sample is taken on the first external clock edge after startup.

Using the Input Trigger with External Input Clocking

Input triggering may be used with external input clocking. When these functions are used together, however, precise synchronization of acquisition to a trigger edge is not available. The reason for the loss of synchronization is that the Data Acquisition Processor has no control over the external clock.

For the DAP 800, DAP 1200e, and DAP 2400e, the time from a trigger edge until the first conversion will be from 1 to 2 external clock cycles, assuming input sampling has stopped. To guarantee recognition of an external trigger after 1 external clock cycle, the external trigger must meet a setup time of 50 ns to the positive edge of the external clock. Each time a trigger is reasserted after being de-asserted there is a 1 to 2 clock delay before acquisition starts. When a hardware trigger is used with the internal clock, the Data Acquisition Processor synchronizes its clock to the edge of the external trigger so there is no synchronization condition.

The DAP 3200e acts upon the first external clock cycle after the trigger has been asserted, assuming input sampling has stopped. To guarantee recognition of an external trigger, the external trigger must meet a setup time of 50 ns to the positive edge of the external clock.

Using the Output Trigger with External Output Clocking

Output triggering may be used with external output clocking. Unlike input clocking, updates can occur on the first external clock after the trigger is asserted. To guarantee recognition of an external clock, the external trigger must meet a setup time of 50 ns to the positive edge of the external clock.

Timing tables

tSYNCH	200 ns on the DAP 3200e four CPU clock cycles on all other models	Time needed to synchronize an internal clock to an external clock
tTRIG_MIN	60 ns	Minimum high period for the input and output trigger
tEXTCLK_PW	25 ns	Minimum high or low period of an external clock
tTCSETUP	50 ns	External trigger to external clock setup time
tITRIG_MAX	250 ns	Maximum high period of the input trigger to guarantee a single conversion
tINSKEW	200 ns	Time from input clock or trigger to conversion value held
tOUTSKEW	30 ns	Time from output clock until start of DAC slewing

9. Cabling for Interface Boards

Microstar Laboratories provides several interface boards for input and output expansion and signal termination. The following chapters describe each interface board in detail. Interface boards are connected to a Data Acquisition Processor using one or more cables from Microstar Laboratories. The following table shows the cables that connect each termination and expansion board to a Data Acquisition Processor:

Board	Uses Cable	
MSTB 003-01 Analog Termination Board	MSCBL 006-01 40 line ribbon	
MSTB 004-01 40-Pin Digital Termination Board	MSCBL 006-01 40 line ribbon	
MSTB 005-01 DAP 800 Termination Board	MSCBL 030-01 50 line ribbon	
MSTB 006-01 BNC Termination Board	MSCBL 006-01 40 line ribbon	
MSTB 008-01 Digital Termination Board	MSCBL 036-01 100 line ribbon	
MSTB 009-01 DAP 1216e/2416e Analog Termination Board	MSCBL 040-01 68 line round cable	
MSXB 001-01 and MSXB 002-01 Analog Input Expansion Board	MSCBL 006-01, 40 line ribbon	MSCBL 014-01 10 line ribbon
MSXB 010-01 4 Input Simultaneous Sampling Board	MSCBL 006-01, 40 line ribbon	MSCBL 014-01 10 line ribbon
MSXB 011-01 16 Input Simultaneous Sampling Board	MSCBL 006-01, 40 line ribbon	MSCBL 014-01 10 line ribbon

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Board	Uses Cable	
MSXB 013-01 Digital Expansion Board	MSCBL 036-01 100 line ribbon	
MSXB 014-01 Analog Output Expansion Board	MSCBL 036-01 100 line ribbon	
MSXB 015-01 Counter/Timer Board	MSCBL 036-01 100 line ribbon	
MSXB 016-01 Opto-Isolator Board	MSCBL 036-01 100 line ribbon	
MSXB 017 5B Analog Isolation Board	MSCBL 006-01, 40 line ribbon	MSCBL 014-01 10 line ribbon
MSXB 018-01 Analog Input Expansion Board For DAP 1216e and DAP 2416e	MSCBL 040-01 68 line round cable	
MSXB 019-01 DAP 800 Analog Input Expansion Board	MSCBL 030-01 50 line ribbon	
MSXB 020-01 e Series Analog Output Expansion Board	MSCBL 006-01, 40 line ribbon	MSCBL 014-01 10 line ribbon
MSXB 021-01 DAP 800 Analog Termination Expansion	MSCBL 030-01 50 line ribbon	
MSXB 022-01 16-bit Analog Output Expansion Board	MSCBL 036-01 100 line ribbon	
MSXB 023-01 Quadrature Decoder Board	MSCBL 036-01 100 line ribbon	

10. Analog Termination Board

The Microstar Laboratories Analog Termination Board, part number MSTB 003-01, is a 40-point quick connect termination board for analog signals. It provides access to all connections on the Data Acquisition Processor analog connector. The Analog Termination Board provides a ground connection for each input and output signal, allowing easy connection to discrete devices.

All input connections are labeled with both the signal name and the pin number of the 40-pin connector on the Data Acquisition Processor. The pin numbers are discussed in the connector chapters earlier in this manual. The Analog Termination Board comes from the factory configured for voltage input. It can be configured for current input or for input voltages that exceed Data Acquisition Processor specifications. The Analog Termination Board also has an area for wire wrapping custom circuits.

The Analog Termination Board also can be used for differential inputs. A differential input is used to measure the difference between two voltages. The negative terminal voltage is subtracted from the positive terminal voltage. When a differential voltage is measured, a ground sense line must be connected between the Analog Termination Board and the signal source. Table 1 shows the correspondence between differential and single-ended inputs.

Table 1.

Single-Ended Input	Differential Input
S0	D0-
S1	D0+
S2	D1-
S3	D1+
S4	D2-
S5	D2+
S6	D3-
S7	D3+
S8	D4-
S9	D4+
S10	D5-
S11	D5+
S12	D6-
S13	D6+
S14	D7-
S15	D7+

The Data Acquisition Processor digital-to-analog converter outputs are available on the Analog Termination Board, along with ground returns for both outputs. The output current from each digital-to-analog converter output is rated at ± 5 milliamps, but it is recommended that this current not exceed ± 1 milliamp. The digital-to-analog converter outputs are voltage outputs.

The Data Acquisition Processor also has ± 15 volt supply voltages; these are available on the Analog Termination Board. The maximum allowable current drain from these supplies is 50 milliamps per side. If more current than this is required, an external power supply is necessary.

Hardware Configuration

The Analog Termination Board is connected to a Data Acquisition Processor using a 40-line ribbon cable, part number MSCBL 006-01. MSCBL 006-01 connects the analog connector of a Data Acquisition Processor to connector `J1` of the Analog Termination Board. The input signal connections on the Analog Termination Board are labeled `S1`, `S2`, etc. The input ground connections are labeled `G1`, `G2`, etc.

Note: If the Data Acquisition Processor does not have fault-protected input multiplexers, signals must not be applied to the termination board when power is not applied to the Data Acquisition Processor.

Current Input

To configure a current input, place a resistor in the location on the termination board corresponding to the input pin being reconfigured. Figure 9 and Table 2 show resistor placement. The appropriate size for this resistor can be calculated using Ohms law, given the maximum input current and the input voltage range of the Data Acquisition Processor.

```
Ohm's Law: Resistance = Voltage / Current
```

The Data Acquisition Processor is shipped from the factory with an input range of +/- 5 volts. The accuracy of the measurements made in this configuration depends on the precision of the resistors used and this should be taken into consideration when selecting the resistors. Microstar Laboratories recommends using resistors with a 1% or better tolerance.

Excess power dissipated in the resistor causes heating; this changes the resistance value, decreasing the accuracy of the measurements. The recommended maximum power dissipation is 0.1 watt.

```
Power Calculation: Power = current² * resistance
```

For current input, a current source is connected to the `Sx` terminal and the ground return is connected to the `Gx` terminal. To convert voltage input `S0` into a current input that generates 1 to 5 volts with an input current of 4 to 20 milliamps, a 250 ohm resistor is inserted in the `R31` location. In this case, the maximum power dissipated in the resistor is 0.1 watt at +5 volts; this is the maximum recommended power dissipation. Figure 7 illustrates the connections for this example.

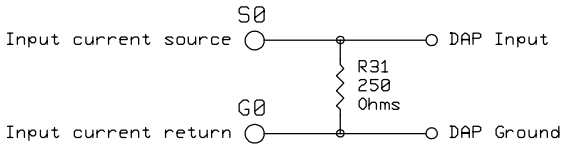

Figure 7.

Voltage Divider

The termination board can be configured for applications requiring input voltages greater than that allowed by the Data Acquisition Processor. This is accomplished by soldering a resistive voltage divider in the location provided on the termination board. Before this can be done, a trace on the termination board must be cut. Above each even numbered resistor there is a row of five small holes. Between two of the holes there is a white "X". The trace at the X must be cut.

Once this trace is cut, the resistors for the voltage divider are soldered into place. The resistor on the ground side of the divider is placed in an odd numbered resistor location and the resistor on the input signal side of the divider is placed in an even numbered resistor location. Figure 9 and Table 2 illustrate resistor placement for each input.

After both resistors are soldered into place, signals may be connected between the Sx and Gx terminals. Test the voltage divider circuit before connecting the circuit to the Data Acquisition Processor.

Note: Be careful to avoid applying an input voltage that exceeds Data Acquisition Processor specifications.

Warning: If the trace on the termination board is not cut, the high voltage input is connected directly to the Data Acquisition Processor input; this may destroy the Data Acquisition Processor.

For example, to configure input S0 so that an input range of 0 to 20 volts is scaled down to a range of 0 to 5 volts, a resistor ratio of 3:1 is needed.

Voltage Divider Equation: $V_{out} = V_{in} * R1/(R1+R2)$

Resistance values of 1500 and 500 ohms may be used. The trace beneath the X above R32 is cut. Then the 500 ohm resistor is placed in the R31 position and the 1500 ohm resistor is placed in the R32 position. Since 500 ohm resistors are not commonly available, a 510 ohm resistor would typically be used instead, resulting in a small error in the division ratio. This error is linear and can be corrected by multiplying by a constant in DAPL. Figure 8 illustrates the circuit for this example.

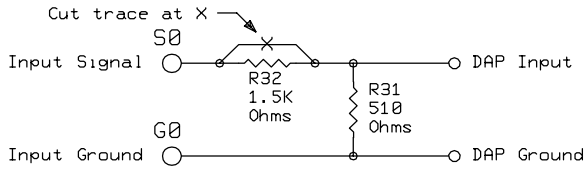

Figure 8.

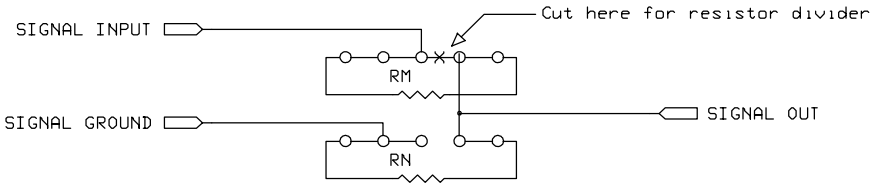

Figure 9.

Note: To avoid exceeding Data Acquisition Processor input voltage specifications, make sure both resistors are securely soldered in the correct locations and the trace beneath the X is completely cut before using the circuit.

Table 2.

Terminal	Current Input Resistor *	Voltage Divider Resistors
S0, G0	R31	R31, R32
S1, G1	R29	R29, R30
S2, G2	R27	R27, R28
S3, G3	R25	R25, R26
S4, G4	R23	R23, R24
S5, G5	R21	R21, R22
S6, G6	R19	R19, R20
S7, G7	R17	R17, R18
S8, G8	R15	R15, R16
S9, G9	R13	R13, R14
S10, G10	R11	R11, R12
S11, G11	R9	R9, R10
S12, G12	R7	R7, R8
S13, G13	R5	R5, R6
S14, G14	R3	R3, R4
S15, G15	R1	R1, R2

* The current input resistor is placed in the RN location shown in the previous figure.

** The first resistor is on the ground side of the voltage divider (RN), the second is on the input signal side (RM), as shown in the previous diagram. For example, R31 is RN and R32 is RM. Figure 9 shows the resistor placement.

Table 2 and Figure 9 can be used to locate the appropriate resistors when using either the current input or voltage division configuration. Figure 9 shows schematically how the inputs and grounds on the termination board are connected.

Cold Junction Reference

The analog termination board, part number MSTB 003-02, has a cold junction reference circuit. This circuit is used to measure the temperature of the 'cold junction' at the termination board. Since the cold junction temperature is the same for all thermocouples connected to a termination board, only one cold junction reference circuit is needed for any number of thermocouples.

The cold junction reference circuit generates a differential voltage which is temperature dependent. The outputs of this circuit are connected to differential input `D4` of the termination board. The Data Acquisition Processor samples this voltage and the resultant information is used in the `THERMO` command for cold junction compensation.

Note: When the cold junction reference circuit is installed, no other inputs should be connected to the `S8` and `S9` terminals, as they are connected to the cold junction reference circuit.

Figure 10 shows the cold junction reference circuit.

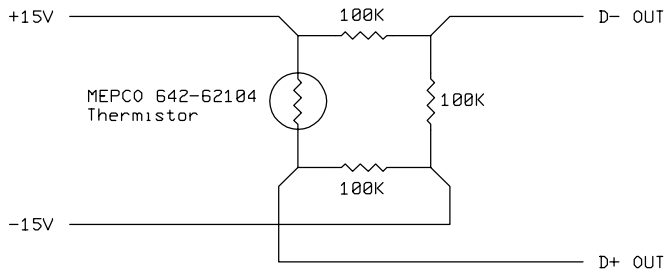

Figure 10.

The following table shows the relationship between output voltage and temperature.

Voltage (V)	Temperature (C)
-5.000	10.86
-4.000	13.78
-3.000	16.63
-2.000	19.43
-1.000	22.21
0.000	25.00
1.000	27.85
2.000	30.71
3.000	33.68
4.000	36.78
5.000	40.04

11. MSTB 004 Digital Termination Board 40-Pin

The Microstar Laboratories Digital Termination Board, part number MSTB 004-01, is a 72-point quick connect termination board for digital signals. It provides access to the digital I/O connector of older Data Acquisition Processor boards with 40-pin digital connectors. The Digital Termination Board also provides ground reference connections and +5 volt and ground power connections.

Hardware Configuration

The Digital Termination Board is connected to the Data Acquisition Processor with one 40-line ribbon cable, part number MSCBL 006-01. This cable connects `J1` of the Digital Termination Board to `J1` of the Data Acquisition Processor.

Note: The Digital Termination Board should not be connected or disconnected while the Data Acquisition Processor is powered.

All input connections are labeled `DIx` where `x` is the input number; `x` ranges from 0 to 15. Each input connection has an adjacent ground connection. The inputs are ALS TTL; they sink no more than 20 microamps for a “1” input and source no more than 0.2 milliamps for a “0” input. An input voltage greater than 2V is interpreted as a “1” and an input voltage less than 0.8V is interpreted as a “0”.

Digital input pins may have signals applied when the Data Acquisition Processor is off.

Note: If a voltage greater than 5V or less than 0V is applied to an input, damage to the Data Acquisition Processor may occur.

All output connections on the Digital Termination Board are labeled `DOx` where `x` is the output number; `x` ranges from 0 to 15. Each output has an adjacent ground connection. The outputs are ALS TTL; they can sink no more than 24 milliamps for a “0” output and can source no more than 2.6 milliamps for a “1” output. The output voltage for a “1” is at least 2.6V and the output voltage for a “0” is less than 0.5V.

All ground connections are electrically connected on the Digital Termination Board, and are connected to the Data Acquisition Processor ground. All signals connected to a Digital Termination Board must share the PC’s ground as a common reference.

Note: If the output current is extended beyond maximum ratings, damage to the Data Acquisition Processor is possible.

The Data Acquisition Processor internal input clock output is available on the Digital Termination Board; this output is labeled CLK. The digital input expansion bits are available on connections labeled DXA, DXB, and DXC.

The Digital Termination Board also has connections for the Data Acquisition Processor +5V power supply. The 5V supply has two connections on the Digital Termination Board; the 5V supply current is rated at 500 milliamps per connection.

12. MSTB 006 BNC Termination Board

The Microstar Laboratories BNC Termination Board, part number MSTB 006-01, is an 18 BNC connector termination board for analog signals. It provides access to all analog inputs and outputs on the Data Acquisition Processor analog connector.

All connections are labeled with the signal name corresponding to the connections of the 40-pin analog connector on the Data Acquisition Processor. See the connector chapters for more information on the connector pins. The BNC Termination Board provides positions for mounting termination resistors and provides an area for wire wrapping custom circuits.

Note: The BNC Termination Board should not be connected or disconnected while the Data Acquisition Processor is powered.

The BNC Termination Board can be used for differential inputs. A differential input is used to measure the difference between two voltages. The negative terminal voltage is subtracted from the positive terminal voltage. When a differential voltage is measured, a ground sense line must be connected between the BNC Termination Board and the signal source. Table 3 shows the correspondence between differential and single-ended inputs.

Table 3.

Single-Ended Input	Differential Input
S0	D0-
S1	D0+
S2	D1-
S3	D1+
S4	D2-
S5	D2+
S6	D3-
S7	D3+
S8	D4-
S9	D4+
S10	D5-
S11	D5+
S12	D6-
S13	D6+
S14	D7-
S15	D7+

The Data Acquisition Processor digital-to-analog converter outputs are available on the BNC Termination Board, along with ground returns for both outputs. The current from each digital-to-analog converter output is rated at ± 5 milliamps but it is recommended that this current not exceed ± 1 milliamp. The digital-to-analog converter outputs are voltage outputs.

Hardware Configuration

The BNC Termination Board is connected to a Data Acquisition Processor using a 40-line ribbon cable, part number MSCBL 006-01. MSCBL 006-01 connects the analog connector of a Data Acquisition Processor to connector `J1` of the Analog Termination Board. The input signal connections on the BNC Termination Board are labeled `S1`, `S2`, etc.

Note: If the Data Acquisition Processor does not have fault-protected input multiplexers, signals must not be applied to the termination board when power is not applied to the Data Acquisition Processor.

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13. MSXB 002 Analog Input Expansion Board

The Microstar Laboratories Analog Input Expansion Boards multiplex 64 analog inputs into a Data Acquisition Processor. As many as eight Analog Input Expansion Boards can be connected to a Data Acquisition Processor to provide up to 512 analog inputs.

Hardware Configuration

An Analog Input Expansion Board is connected to a Data Acquisition Processor using two cables, MSCBL 006-01 and MSCBL 014-01. MSCBL 006-01 is a 40-line ribbon cable which connects the analog connector of the Data Acquisition Processor to connector `J1` of the Analog Input Expansion Board. MSCBL 014-01 is a 10-line ribbon cable which connects the analog expansion connector of the Data Acquisition Processor to connector `J6` of the Analog Input Expansion Board.

Note: The Analog Input Expansion Board should not be connected or disconnected while the Data Acquisition Processor is powered.

Connectors `J2`, `J3`, `J4`, and `J5` of the Analog Input Expansion Board accept 64 single-ended or 32 differential analog input signals. These 40-pin connectors have the same pinout as the Data Acquisition Processor analog connector, with ground lines adjacent to the signal lines. Signals may be connected to an Analog Input Expansion Board using either Analog Termination Boards, part number MSTB 003-01, or 40 wire cable kits, part number MSCBL 004-01K.

The inputs pins of the Analog Input Expansion Board are ordered differently than the input pins specified in DAPL `SET` commands. Use the following tables to map the DAPL input pins to the corresponding Analog Input Expansion Board input pins.

Single-Ended Inputs

DAPL Input Pin	Connector	Connector Pin	Corresponding Termination Board Label
S0	J5	39	S0
S1	J5	38	S1
S2	J5	31	S8
S3	J5	30	S9
S4	J4	39	S0
S5	J4	38	S1
S6	J4	31	S8
S7	J4	30	S9
S8	J3	39	S0
S9	J3	38	S1
S10	J3	31	S8
S11	J3	30	S9
S12	J2	39	S0
S13	J2	38	S1
S14	J2	31	S8
S15	J2	30	S9
S16	J5	37	S2
S17	J5	36	S3
S18	J5	29	S10
S19	J5	28	S11
S20	J4	37	S2
S21	J4	36	S3
S22	J4	29	S10
S23	J4	28	S11
S24	J3	37	S2
S25	J3	36	S3
S26	J3	29	S10
S27	J3	28	S11
S28	J2	37	S2
S29	J2	36	S3
S30	J2	29	S10
S31	J2	28	S11

Single-Ended Inputs, Continued

DAPL Input Pin	Connector	Connector Pin	Corresponding Termination Board Label
S32	J5	35	S4
S33	J5	34	S5
S34	J5	27	S12
S35	J5	26	S13
S36	J4	35	S4
S37	J4	34	S5
S38	J4	27	S12
S39	J4	26	S13
S40	J3	35	S4
S41	J3	34	S5
S42	J3	27	S12
S43	J3	26	S13
S44	J2	35	S4
S45	J2	34	S5
S46	J2	27	S12
S47	J2	26	S13
S48	J5	33	S6
S49	J5	32	S7
S50	J5	25	S14
S51	J5	24	S15
S52	J4	33	S6
S53	J4	32	S7
S54	J4	25	S14
S55	J4	24	S15
S56	J3	33	S6
S57	J3	32	S7
S58	J3	25	S14
S59	J3	24	S15
S60	J2	33	S6
S61	J2	32	S7
S62	J2	25	S14
S63	J2	24	S15

Differential Inputs

DAPL Input Pin	Connector	Connector Pin	Corresponding Termination Board Label
D0	J5	39, 38	D0
D1	J5	31, 30	D4
D2	J4	39, 38	D0
D3	J4	31, 30	D4
D4	J3	39, 38	D0
D5	J3	31, 30	D4
D6	J2	39, 38	D0
D7	J2	31, 30	D4
D8	J5	37, 36	D1
D9	J5	29, 28	D5
D10	J4	37, 36	D1
D11	J4	29, 28	D5
D12	J3	37, 36	D1
D13	J3	29, 28	D5
D14	J2	37, 36	D1
D15	J2	29, 28	D5
D16	J5	35, 34	D2
D17	J5	27, 26	D6
D18	J4	35, 34	D2
D19	J4	27, 26	D6
D20	J3	35, 34	D2
D21	J3	27, 26	D6
D22	J2	35, 34	D2
D23	J2	27, 26	D6
D24	J5	33, 32	D3
D25	J5	25, 24	D7
D26	J4	33, 32	D3
D27	J4	25, 24	D7
D28	J3	33, 32	D3
D29	J3	25, 24	D7
D30	J2	33, 32	D3
D31	J2	25, 24	D7

Mapping Input Pins

DAPL provides an option that maps the pins of an Analog Input Expansion Board so they match the order on the Data Acquisition Processor analog connector. Use the DAPL command `OPTION AINEXPAND=ON` to set DAPL so that it automatically maps the Analog Input Expansion Board input pins to the input pins of the `SET` command. When `AINEXPAND` is on, the `SET` command maps to the Analog Input Expansion Board as shown in the following table:

DAPL Input Pins	Analog Input Expansion Board Pins
S0 ... S15	`J5: S0 . S15`
S16 ... S31	`J4: S0 . S15`
S32 ... S47	`J3: S0 . S15`
S48 ... S63	`J2: S0 . S15`
D0 ... D7	`J5: D0 . D7`
D8 ... D15	`J4: D0 . D7`
D16 ... D23	`J3: D0 . D7`
D24 ... D31	`J2: D0 . D7`

For inputs `S64` and above, the pin sequence repeats.

Sampling Speed with External Expansion

When using external expansion, the multiplexer settling time must be added to the settling time of the on-board analog circuits. This is restrictive only at very high sampling speeds.

Software Configuration

DAPL automatically generates expansion control signals, as specified by input procedure SET commands. For example, the following input procedure reads from expanded analog inputs:

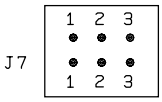
```
RESET
   IDEF A 5
   SET IPIPE0 S0
   SET IPIPE1 S57
   SET IPIPE2 D23
   SET IPIPE3 D4
   SET IPIPE4 D18 100
   TIME 10000
   END
PDEF B
   PRINT
   END
START A, B
```

More Than One Analog Input Expansion Board

Several Analog Input Expansion Boards can be connected together to provide additional input expansion. When more than one Analog Input Expansion Board is used, the J1 and J6 connectors of all Analog Input Expansion Boards are tied together. Contact Microstar Laboratories for information about special cables which provide this feature.

Up to eight Analog Input Expansion Boards can be connected to an e-Series board. No external power is required. For the DAP 2400, eight standard Analog Input Expansion Boards or three protected expansion boards can be connected without external power.

Each Analog Input Expansion Board must be configured to recognize a specific input pin range. Connector J7 selects this range.

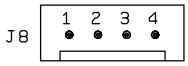


The bottom of connector J7 is closest to connector J8. The input pin range is selected by adding an offset according to the following table:

Single-Ended Input Range	Differential Input Range	Board Number	Jumpers
0 - 63	0 - 31	0	1, 2, 3
64 - 127	32 - 63	1	1, 2
128 - 191	64 - 95	2	1, 3
192 - 255	96 - 127	3	1
256 - 319	128 - 159	4	2, 3
320 - 383	160 - 191	5	2
384 - 447	192 - 223	6	3
447 - 511	224 - 255	7	none

External Trigger Connection

An external trigger signal can be connected to connector J8 of the Analog Input Expansion Board to provide hardware triggering. See the connector chapters and Chapter 8 for more information about hardware triggering. The pinout of connector J8 is:



The top of connector J8 is closest to the connector marked J7. Pins 1 and 3 are digital ground and pin 4 is the external trigger input. Pin 2 is connected to pin 2 of the Data Acquisition Processor analog control connector which is the external input clock. External signals connected to J8 must be in the standard TTL range of 0 to +5 volts. The pins on J8 connect directly to the pins on a Data Acquisition Processor.

14. MSXB 010/011 Simultaneous Sampling Board

The Simultaneous Sampling Board acquires up to 16 analog signals simultaneously, allowing a Data Acquisition Processor to acquire multi-input data without the time skew usually associated with multiplexed data acquisition systems. Three models of Simultaneous Sampling Boards currently are available from Microstar Laboratories; their part numbers are MSXB 011-01, MSXB 011-02, and MSXB 010-01.

MSXB 011-01 acquires up to 16 signals simultaneously. The Simultaneous Sampling Board allows expansion to more than 16 inputs. MSXB 011-02 is the same as the MSXB 011-01 and provides connections for external power when more than 2 boards are used. MSXB 010-01 acquires up to four signals simultaneously. Also, MSXB 010-01 provides 12 non-simultaneous analog inputs. The MSXB 011-01 should be used when additional expansion is required.

Hardware Configuration

A Simultaneous Sampling Board is connected to a Data Acquisition Processor using two cables, MSCBL 006-01 and MSCBL 014-01. MSCBL 006-01 is a 40-line ribbon cable which connects the analog connector of a Data Acquisition Processor to connector `J2` of a Simultaneous Sampling Board. MSCBL 014-01 is a 10-line ribbon cable which connects the analog expansion connector of a Data Acquisition Processor to connector `J3` of a Simultaneous Sampling Board.

Note: Both cables always must be connected between the Simultaneous Sampling Board and the Data Acquisition Processor; damage may occur if only one cable is connected. Never connect or disconnect either of the cables joining a Simultaneous Sampling Board and a Data Acquisition Processor while power is applied to the Data Acquisition Processor.

Connector `J1` of the Simultaneous Sampling Board accepts analog input signals. This 40-pin connector has the same pinout as the Data Acquisition Processor analog connector. For MSXB 010-01, `S0-S3` are simultaneously sampled inputs; `S4-S15` are non-simultaneous inputs.

The analog inputs of the Simultaneous Sampling Board may have voltages applied when power is on or off. Maximum allowable input voltage is +/- 15 volts.

Software Configuration

The signals from a Simultaneous Sampling Board appear to DAPL in two input pin ranges, each consisting of either 16 single-ended input pins or 8 differential input pins. Any combination of single-ended or differential inputs may be used. Selecting any input in the lower address range (`S0-S255`) places all of the boards into hold mode; selecting any input in the upper address range (`S256-S511`) places all of the boards into track mode. As shipped from Microstar Laboratories, a Simultaneous Sampling Board occupies the input pins `S0 - S15` (`D0 - D7`).

Reading from any pin in the address range above 255 places all the sample and hold amplifiers on all the Simultaneous Sampling Boards into track mode. This is a dummy reading and the value from this input channel pipe should be ignored. Reading from any pin in the lower address range of 0 to 255 gives a value corresponding to the input signal, as held on the last transition from track mode to hold mode.

An input procedure for acquiring signals simultaneously usually includes one `SET` command addressing an input pin in the upper address range, followed by several `SET` commands addressing the pins to be sampled.

The following is a typical input procedure definition. The input procedure `A` acquires the signals on `S0` and `S1` simultaneously. A `FORMAT` command sends the input data to the PC:

```
RESET
IDEF A 3
   SET IPIPE0 S256
   SET IPIPE1 S0
   SET IPIPE2 S1
   TIME 1000
   END
PDEF B
   FORMAT(IPIPE1, IPIPE2)
   END
START A, B
```

Note that data from input channel pipe 0 are ignored. The only function of the `SET IPIPE0 S256` command is to place the Simultaneous Sampling Board into track mode.

Notes:

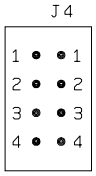
- At a gain of 1 all signals must be converted within 10,000 µs of the transition from track to hold.
- At a gain of 10 all signals must be converted within 1,000 µs of the transition from track to hold.
- The Simultaneous Sampling Boards should not be used at gains greater than 10.
- Readings in track mode show small offsets from the corresponding readings in hold mode. This is normal, as offset compensation is adjusted only for hold mode.
- The Simultaneous Sampling Board must be held in track mode for a minimum of 12 µs before switching to hold mode. This is to provide adequate settling time for large voltage swings.

More Than One Simultaneous Sampling Board

Several MSXB 011-01 boards can be connected together to provide simultaneous acquisition of more than 16 inputs. When more than one Simultaneous Sampling Board is used, the J2 and J3 connectors of all Simultaneous Sampling Boards are tied together. Contact Microstar Laboratories for information about special cables which provide this feature. External power is required when more than 2 Simultaneous Sampling Boards are used.

Note that the MSXB 010-01 does not have on-board circuitry for expansion. It can be expanded with the use of an Analog Input Expansion Board. The MSXB 011-01, however, has expansion circuitry and should be used when more than four simultaneous inputs are needed.

Each MSXB 011-01 must be configured to recognize a specific input pin range. The range is selected by J4, a header of two rows on .100 inch centers. Connector J4 is located above the DC-to-DC converter and below J2.



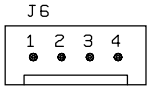
The input pin ranges are specified in the following table:

Single-ended Hold mode	Differential Hold mode	Board Number	Jumpers
0 - 15	0 - 7	0	1, 2, 3, 4
16 - 31	8 - 15	1	1, 2, 3
32 - 47	16 - 23	2	1, 2, 4
48 - 63	4 - 31	3	1, 2
64 - 79	32 - 39	4	1, 3, 4
80 - 95	40 - 47	5	1, 3
96 - 111	48 - 55	6	1, 4
112 - 127	56 - 63	7	1
128 - 143	64 - 71	8	2, 3, 4
144 - 159	72 - 79	9	2, 3
160 - 175	80 - 87	10	2, 4
176 - 191	88 - 95	11	2
192 - 207	96 - 103	12	3, 4
208 - 223	104 - 111	13	3
224 - 239	112 - 119	14	4
240 - 255	120 - 127	15	none

Connector J9 enables the address on J4. J9 is located to the right of J4. J9 should have a jumper installed when several Simultaneous Sampling Boards are used. When J9 does not have a jumper, the Simultaneous Sampling Board is enabled independently of the address provided by the Data Acquisition Processor.

External Trigger Connection

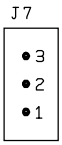
An external trigger signal can be connected to connector J6 to provide hardware triggering. See the Chapter 8 for more information about hardware triggering. J6 is a header of one row on .100 inch centers. The connector J6 is Molex part number 22-23-2041. J6 is located near connector J3.



Pins 1 and 3 are digital ground and pin 4 is the external trigger input. Pin 2 is connected to pin 2 of the Data Acquisition Processor analog control connector. When the Simultaneous Sampling Board is connected to a Data Acquisition Processor, pin 2 is the external input clock. External signals connected to J6 must be in the standard TTL range of 0 to +5 volts. The pins on J6 connect directly to the pins on a Data Acquisition Processor.

External Power Connections

On MSXB 011-02, connector J7 provides connection for external power when more than two Simultaneous Sampling Boards are used. Connector J7 is a single row header on .156 inch centers. J7 is located above the DC to DC converter and to the right of connector J9. J7 is Molex part number 26-60-4030. It mates with 09-50-3031. MSXB 011-02 requires 1.0 Amp power.



Pin 1 of connector J7 is +5 volt input, pin 2 is ground and pin 3 is not used.

Note: It is best to power the MSXB 011-02 from the host PC's power supply so that both the MSXB 011-02 and the Data Acquisition Processor are powered on and off at the same time. If this is not practical, then external power to the MSXB 011-02 should be applied before powering on the Data Acquisition Processor and should be disconnected after powering off the Data Acquisition Processor.

15. MSXB 017 5B Analog Isolation Board

The Microstar Laboratories 5B Analog Isolation Board, part number MSXB 017, provides an isolated analog interface to the DAP 1200e, DAP 2400e, and DAP 3200e. Isolation is available for analog inputs as well as analog outputs. Isolation protects the Data Acquisition Processor from high voltages and provides the independence from ground that some applications require.

5B series isolated signal conditioning modules provide the isolated analog interface. Input and output modules exist to serve a variety of functions. The 5B Analog Isolation Board has eight channels that can be used for either input or output, depending on the module installed. Up to eight input modules can be installed on each board. Up to four output modules can be installed as discussed below in the output section.

The 5B Analog Isolation Board is compatible with all 5B isolated signal conditioning modules. These modules are available from Microstar Laboratories and other sources.

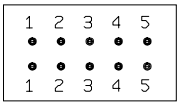
The number of input channels can be expanded to 512 without having to use an Analog Input Expansion Board. The 5B Analog Isolation Board uses the same input expansion addressing scheme as the Analog Input Expansion Board and may be used in conjunction with the Analog Input Expansion Board.

Hardware Configuration

The 5B Analog Isolation Board connects to the Data Acquisition Processor using two cables, MSCBL 006-01 and MSCBL 014-01. MSCBL 006-01 is a 40-line ribbon cable which connects the analog I/O connector of a Data Acquisition Processor to connector `J1` of the 5B Analog Isolation Board. MSCBL 014-01 is a 10-line ribbon cable which connects the analog expansion connector of the Data Acquisition Processor to connector `J2` of the 5B Analog Isolation Board. All outputs from the eight channels on the 5B Analog Isolation Board connect to the lower eight analog single-ended inputs of connector `J1`. Connector `J1` has the same pin-out as the analog I/O connector of the Data Acquisition Processor.

Input Range

Each 5B Analog Isolation Board must be configured to recognize a specific input address range. The jumper setting on connector `J7` selects this range.



J7

Pin 1 of connector `J7` is closest to the bottom edge of the board. The input range is selected according to the following table:

Low Order Input Range	Jumper Setting	High Order Input Range
0 - S7	1, 2, 3, 4, 5	S8 - S15
S16 - S23	1, 2, 3, 4	S24 - S31
S32 - S39	1, 2, 3, 5	S40 - S47
S48 - S55	1, 2, 3	S56 - S63
S64 - S71	1, 2, 4, 5	S72 - S79
S80 - S87	1, 2, 4	S88 - S95
S96 - S103	1, 2, 5	S104 - S111
S112 - S119	1, 2	S120 - S127
S128 - S135	1, 3, 4, 5	S136 - S143
S144 - S151	1, 3, 4	S152 - S159
S160 - S167	1, 3, 5	S168 - S175
S176 - S183	1, 3	S184 - S191
S192 - S199	1, 4, 5	S200 - S207
S208 - S215	1, 4	S216 - S223
S224 - S231	1, 5	S232 - S239
S240 - S247	1	S248 - S255
S256 - S263	2, 3, 4, 5	S264 - S271
S272 - S279	2, 3, 4	S280 - S287
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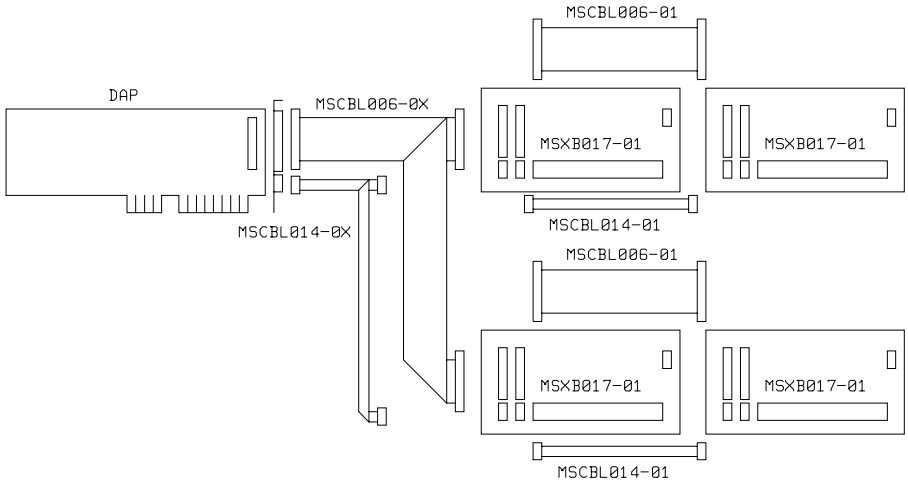
S416 - S423	3, 5	S424 - S431
S432 - S439	3	S440 - S447
S448 - S455	4, 5	S456 - S463
S464 - S471	4	S472 - S479
S480 - S487	5	S488 - S495
S496 - S503	none	S504 - S511

Each jumper setting on connector J7 selects an address range of 16 input channels. There are only eight channels on each 5B Analog Isolation Board, but connector J3 can be used for maximum expandability. Connector J3 is a 40-pin connector that allows a second 5B Analog Isolation Board to share the same input address in a daisy chain. Input channels S0-S7 on J3 are connected to input channels S8-S15 on J1 on the other 5B Analog Isolation Board. Two 5B Analog Isolation Boards can share the same board address by connecting J1 of the second 5B Analog Isolation Board to J3 of the first 5B Analog Isolation Board, and J1 of the first 5B Analog Isolation Board

to the Data Acquisition Processor. The following figure shows a sample setup with four 5B Analog Isolation Boards connected in a daisy chain.



In this setup, the top two boards share one address while the bottom two boards share a different address. The input channels on the left two boards are the low order inputs while the input channels on the right two boards are the high order inputs listed in the table above. For example, if jumper `J7` of the top two boards were set to 1,2,3,4,5 and `J7` of the bottom two boards were set to 2,3,4,5, then the input channels of the top left board would be `S0-S7`; the input channels of the top right board would be `S8-S15`; the input channels of the bottom left board would be `S16-S23`; and the input channels of the bottom right board would be `S24-S31`. Up to 512 inputs are available by connecting 64 5B Analog Isolation Boards in this fashion.

Note: Connecting a third 5B Analog Isolation Board to connector `J3` of the second 5B Analog Isolation Board will not work because the Data Acquisition Processor would not receive any input signals from a third 5B Analog Isolation Board.

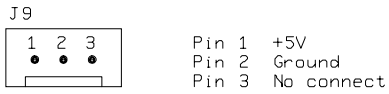
Outputs

Each of the 2 DAC outputs from connector J1 is connected to two of the eight module channels. DAC0 connects to channels 4 and 5 while DAC1 connects to channels 6 and 7. Connector J6 allows four DAC outputs from an Analog Output Expansion Board to be connected. The four DAC outputs from the Analog Output Expansion Board connect to channels 0, 1, 2, and 3. Up to 66 output channels can be used by daisy-chaining 16 5B Analog Isolation Boards and 16 Analog Output Expansion Boards.

External Power

The 5B Analog Isolation Board draws its power from the Data Acquisition Processor's +5V power supply. This supply is limited to 1 Amp. The 5B Analog Isolation Board draws 30 mA alone, without any modules installed. Most 5B modules typically draw 30 mA. Using this estimation, four 5B Analog Isolation Boards can be connected to the Data Acquisition Processor without using external power. The user should check the specifications of the particular 5B modules used, and make sure that the total current drawn from the Data Acquisition Processor does not exceed 1 amp. If the total power consumption exceeds this limit, the MSXB 017-02 model must be used with external power.

The MSXB 017-02 allows connection to an external 5-volt power supply through connector J9. Connector J9 is a male Molex connector part number 26-60-4030 and mates with the Molex connector part number 09-50-3031. Both mating connectors are included with the Microstar Laboratories cable kit MSCBL 027-01K.



Pin 1 is closest to connector J4.

Field Side Interface

The user connects signals to the input/output channels by means of the termination connector J5. Each channel has four terminations, which are labeled: -EX, LO, HI, and +EX. The LO and HI terminals are the differential inputs or outputs. The -EX and +EX terminals are the excitation voltage supplies provided by certain modules, such as strain gauge modules.

CJC

The 5B37 and 5B47 thermocouple modules require a temperature sensor for cold junction compensation (CJC). Integrated CJC sensor modules are provided for each module. The CJC circuit does not affect other types of modules that don't require CJC.

Current Input Resistor

Shunt resistor sockets are provided for measuring input current. A 20-ohm precision shunt resistor is provided with each 5B current input module.

Caution: If high voltages are connected to the 5B Analog Isolation Board, extreme caution should be used to prevent electric shock. Always disconnect all high voltages before handling the 5B Analog Isolation Board. Mount the 5B Analog Isolation Board so that it cannot come into contact with conductive materials.

Overvoltage Protection

The 5B modules provide protection from overvoltages. A typical 5B module provides 240V rms continuous input protection on any of the field side inputs. It also provides 1500V rms common mode input to output isolation. The user should check the specifications of the particular 5B module being used. If there is a danger of exceeding the module's isolation voltage limit, the grounding bolt near connector `J6` should be connected to ground with a large diameter wire that is as short as possible. In the event of module failure, the grounding bolt is used to divert potentially large currents which could damage the Data Acquisition Processor.

16. MSXB 020 Digital Expansion Board

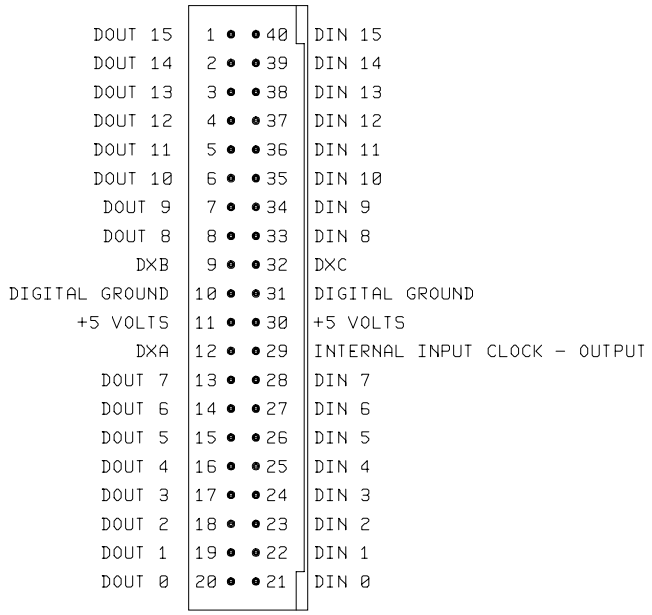
The Microstar Laboratories Digital Input/Output Expansion Board, part number MSXB 020-01, provides the Data Acquisition Processor with 64 digital inputs and 64 digital outputs with 40-pin connectors. By using multiple Digital Input/Output Expansion Boards the Data Acquisition Processor can be expanded to control up to 128 digital inputs and 1024 digital outputs.

Hardware Configuration

A Digital Input/Output Expansion Board is connected to a Data Acquisition Processor using one cable, MSCBL 036-01. MSCBL 036-01 is a 100 line ribbon cable which connects the digital input/output connector of the Data Acquisition Processor to connector `J1` of the Digital Input/Output Expansion Board.

Note: The Digital Input/Output Expansion Board should not be connected to or disconnected from a Data Acquisition Processor while the Data Acquisition Processor is powered.

Each of the connectors `J2`, `J3`, `J4`, and `J5` on the Digital Input/Output Expansion Board accept 16 digital inputs and 16 digital outputs. Connectors `J2`, `J3`, `J4`, and `J5` have the same 40-pin pinout as the DAP 1200 and DAP 2400 digital input/output connector. The pinout of `J2`, `J3`, `J4`, and `J5` is shown on the next page.



Connectors `J2 - J5` correspond to input ports `B0 - B3` and to output ports 0 - 3. The input port name is a parameter of the command `SET`; the output port number is a parameter of the command `DIGITALOUT`.

Signals may be connected to a Digital Input/Output Expansion Board using Digital Termination Boards, part number MSTB 004-01 or a 40 wire cable kit, part number MSCBL 004-01K.

At power up and during reset the outputs of the Digital Input/Output Expansion Board’s expansion ports will track the digital outputs of the Data Acquisition Processor. After power up or a hardware reset the Digital Input/Output Expansion Board's outputs will come up in a known state of either all high or all low depending on the configuration of the Data Acquisition Processor it is connected to. See the Data Acquisition Processor connector chapters for information on how to configure the digital outputs of the Data Acquisition Processor.

Digital inputs

For digital input expansion, DAPL automatically generates expansion control signals, as specified by `SET` commands. The following input procedure reads 16-bit values from the four Digital Input/Output Expansion Board connectors, `J2 - J5`, and sends the values to the PC:

```
RESET
IDEF A 4
   SET IPIPE0 B0
   SET IPIPE1 B1
   SET IPIPE2 B2
   SET IPIPE3 B3
   TIME 10000
   END
PDEF B
   PRINT
   END
START A, B
```

Digital outputs

To use digital output expansion, the DAPL command `OUTPORT` is required. The output port type of the Digital Input/Output Expansion Board is zero.

The following DAPL listing outputs the 16-bit values in pipes `P0 - P3` to the four Digital Input/Output Expansion Board connectors `J2 - J5`:

```
OUTPORT 0..3 TYPE=0

RESET
PIPES P0,P1,P2,P3
PDEF B
   DIGITALOUT(P0, 0)
   DIGITALOUT(P1, 1)
   DIGITALOUT(P2, 2)
   DIGITALOUT(P3, 3)
   END
START B
```

Synchronous Digital Output Expansion

Synchronous digital expansion uses a special protocol which is implemented by the DAPL command `DEXPAND`. For each word of output, the data and address are encoded into four words that are sent to the digital output port. If `DEXPAND` is used, all digital outputs are synchronous on all Digital Input/Output Expansion Boards. See the description of `DEXPAND` in the DAPL manual for more information.

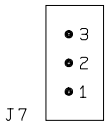
More Than One Digital Input/Output Expansion Board

Several Digital Input/Output Expansion Boards can be connected together to provide additional digital expansion. When more than one Digital Input/Output Expansion Board is used, the `J1` connectors of all Digital Input/Output Expansion Boards are tied together. Contact Microstar Laboratories for information about special cables which provide this feature.

The Digital Input/Output Expansion Board has three socketed termination resistor networks, `RN10`, `RN11` and `RN12`, adjacent to `J1`. The resistors are installed in the sockets when the boards are shipped from the factory. For single board systems, the resistors should remain installed. For multiple board systems, only one board may have the resistors installed. The board farthest from the Data Acquisition Processor should have the resistors installed. If more than one board in a system has the resistors installed, the system may fail.

Input Range

Each Digital Input/Output Expansion Board must be configured to recognize a specific input address range. Connector `J7` selects this range.



Pin 1 of connector J7 is toward the right edge of the Digital Input/Output Expansion Board. The input range is selected according to the following table:

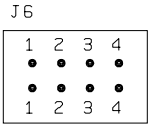
Input Range	Jumper J7
B0-B3	1 to 2
B4-B7	2 to 3
disabled	removed

Each port has 16 binary inputs.

Note: Only two Digital Input/Output Expansion Boards can be used for digital input expansion. If more than two Digital Input/Output Expansion Boards are connected to the Data Acquisition Processor then the Digital Input/Output Expansion Boards not being used for input expansion must have their input expansion disabled by removing the shunt from J7.

Output Range

Each Digital Input/Output Expansion Board must be configured to recognize a specific range of output addresses. Valid address ranges are 0-3, 4-7,…, 60-63. Connector J6 of the Digital Input/Output Expansion Board selects this range.



Pin 1 of connector J6 is closest to the left edge of the Digital Input/Output Expansion Board. The output range is selected according to the following table:

Output Address	Jumpers
0 - 3	1, 2, 3, 4
4 - 7	1, 2, 3
8 - 11	1, 2, 4
12 - 15	1, 2,
16 - 19	1, 3, 4
20 - 23	1, 3
24 - 27	1, 4
28 - 31	1
32 - 35	2, 3, 4
36 - 39	2, 3
40 - 43	2, 4
44 - 47	2
48 - 51	3, 4
52 - 55	3
56 - 59	4
60 - 63	none

Digital output can be expanded past the maximum limit for digital input. For Digital Input/Output Expansion Boards that expand digital output beyond the maximum digital input range, the digital inputs must be disabled by removing the shunt on J7.

17. Recalibration

Each Data Acquisition Processor is burned in and then calibrated by Microstar Laboratories. The accuracy of this calibration should be sufficient for most applications. Accuracy is affected by three factors:

- the operating temperature of the Data Acquisition Processor
- drift in the Data Acquisition Processor circuitry
- analog voltage range selection.

The operating temperature is determined by a number of factors. If the Data Acquisition Processor is operated inside a personal computer, the operating temperature is affected by the number of expansion boards, power supply rating, fan efficiency, etc.

Component drift depends on total operating time of the unit as well as the number of times the unit has been powered up and down.

Changes to analog voltage ranges may require that the Data Acquisition Processor be recalibrated.

For applications requiring high accuracy, occasional recalibration may be necessary. For high absolute accuracy, the Microstar Laboratories calibration sequence requires that measurements be made using a 4.5 digit digital voltmeter with a DC accuracy of .024% (244 ppm) or better. In most applications, only relative accuracy is important, so recalibration with a less accurate digital voltmeter may be acceptable. Calibration also requires a variable voltage source with high stability.

Because calibration requires significant setup time, it generally is best to send Data Acquisition Processors to Microstar Laboratories for recalibration. Calibration is available from Microstar Laboratories for a nominal fee.

CALDAP

CALDAP is a program which uses a PC to recalibrate Data Acquisition Processor analog input circuitry. Recalibration may be necessary if analog voltage range jumpers are changed, or if the Data Acquisition Processor factory calibration has drifted.

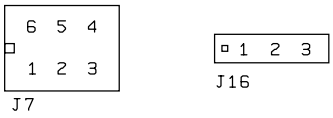
Equipment Requirements

Data Acquisition Processor calibration requires the following equipment:

- A 4 1/2 digit digital voltmeter (DVM).
- A -10 volt to +10 volt adjustable voltage source. The voltage source must be very stable and must have an output impedance of less than 500 ohms.

Connector Numbering

CALDAP prompts refer to particular pins of Data Acquisition Processor connectors. Diagrams with connector locations for each Data Acquisition Processor are included at the beginning of Chapters 4, 5, and 6. Pin 1 of a connector with a single row of pins is identified by a dot, and pin 1 of a connector with two rows of pins is identified by a notch—pins are numbered in a counter-clockwise direction in the same manner as an integrated circuit, as in the following examples:



A PC-bus extender card can be used to permit easier access to the connectors on the Data Acquisition Processor.

Preparing the Data Acquisition Processor

The Data Acquisition Processor must have power applied for at least two hours before calibration.

For a DAP 800, configure the Data Acquisition Processor hardware as follows:

- The S1 (J2:35) pin is connected to the G1 (J2:16) pin.
- The adjustable voltage source is applied across S0 (J2:36) and G0 (J2:15).
- The DVM is connected to sense S0 at (J2:36,J2:15).
- The S7 (J2:29)pin is connected to the S6 (J2:30) pin. These two pins also are connected to DAC1 OUT (J2:28).

For a DAP 1200e, DAP 2400e, or DAP 3200e, configure the Data Acquisition Processor hardware as follows:

- The S1 (J2:38) pin is connected to the G1 (J2:3) pin.
- The adjustable voltage source is applied across S0 (J2:39) and G0 (J2:2).
- The DVM is connected to sense S0 at (J2:39,J2:2).
- The S15 (J2:24) pin is connected to the S14 (J2:25) pin. These two pins also are connected to DAC1 OUT (J2:23).

Starting CALDAP

CALDAP is included on the Data Acquisition Processor diskettes in the subdirectory `\DAP\CALDAP`. Calibration files for the DAP 1200e, the DAP 2400e, the DAP 3200e/101 and the DAP 3200e/102 are in subdirectory `\DAP\CALDAP\DAP2400E`. Calibration files for the DAP 3200e/111, DAP 3200e/214, DAP 3200e/315 and the DAP 3200e/415 are in subdirectory `\DAP\CALDAP\DAP3201E`. Calibration files for the DAP 800 and DAP 801 are in subdirectory `\DAP\CALDAP\DAP800`. The active drive and the active directory should be set so that the CALDAP program is in the current directory. For example:

```
C:
CD \DAP\CALDAP
```

CALDAP should be started by typing CALDAP at the DOS prompt. CALDAP accepts five optional switches:

```
CALDAP [/CF:aaaa\bbbb] [/Rxyz] [/FORCECAL] [/Scccc] [/M]
```

The parameter `aaaa` selects the board type. The board types are as follows:

DAP 800	DAP 800/102, DAP 800/103, DAP 801/101
DAP 2400e	DAP 1200e/4, DAP 1200e/6 DAP 2400e/4, DAP 2400e/5, DAP 2400e/6
DAP 3201e	DAP 3200e/111, DAP 3200e/214, DAP 3200e/315, DAP 3200e/415

The parameter `bbbb` selects the type of calibration. The calibration types are:

`BIP`	Bipolar input range amplifier calibration (DAP 800 only)
`UNI`	Unipolar input range amplifier calibration (DAP 1200e, DAP 2400e, DAP 3200e/101 and DAP 3200e/102 only)
`RANGE`	± 5V input range amplifier calibration (DAP 3200e/111, DAP 3200e/214, DAP 3200e/315 and DAP 3200e/415 only)
`PGA`	PGA gain calibration
`DACS`	DAC calibration
`CAL`	Complete calibration procedure

For the DAP 800, the Bipolar input range calibration is the only calibration required when a bipolar input voltage range jumper selection is changed. For a DAP 1200e, DAP 2400e, or DAP 3200e, the entire calibration sequence is required when the input voltage range is changed. The PGA gain calibration trims the 10, 100, and 500 (1,000

on the DAP 800) gains of the programmable gain amplifier. The DAC calibration calibrates the offsets and gains of the digital-to-analog converters. The complete calibration performs each of the above operations, as well as calibration of the instrumentation amplifier. Microstar Laboratories recommends that a complete calibration not be performed unless specifically required. Calibration is available from Microstar Laboratories for a nominal fee.

The second CALDAP parameter determines calibration voltage ranges. The parameters `x`, `y`, and `z` are numbers selecting voltage ranges. The `x` parameter selects the analog input voltage range:

1 -2.5 to +2.5 volts (DAP 800 only)
2 -5 to +5 volts
3 -10 to +10 volts

The `y` and `z` parameters select the analog output voltage ranges of `DAC0` and `DAC1`, respectively:

1 0 to +10 volts
2 -5 to +5 volts
3 -10 to +10 volts

For example, the following CALDAP command performs complete Data Acquisition Processor calibration with a -10 to +10 volt analog input range and a -10 to +10 volt analog output range on both DACs:

```
CALDAP /CF:DAP2400E\CAL /R333
```

If no range parameter is specified on the CALDAP command line, `/R222` is assumed.

The `/FORCECAL` parameter causes calibration to start immediately upon entry into CALDAP.

The `/Scccc` parameter is for custom Data Acquisition Processors. This parameter should not be specified on the CALDAP command line for normal Data Acquisition Processors. Contact Microstar Laboratories for information on calibrating Data Acquisition Processors with custom analog input sections.

The `/M` parameter is used internally by Microstar Laboratories and should not be specified on the CALDAP command line.

Calibrating the Data Acquisition Processor

Once the PC is executing CALDAP, a `<Ctrl-E>` command from the keyboard is used to begin calibration. This is not necessary if the `/FORCECAL` parameter is used, in which case calibration begins automatically.

CALDAP performs a series of calibration steps. Each calibration step has a unique step number. There are several different types of calibration steps:

1. Configuration step. This step sends configuration information to the Data Acquisition Processor . No user interaction is required.

2. Prompt step. This step waits for you to perform a specific action. The action may be changing a jumper or may be changing the voltage of the variable voltage source. When CALDAP prompts to change the variable voltage, the jumper pin numbers to use for the signal and the ground sense of a `DVM` are provided within parentheses. For example, a prompt of `Inst Out (J7:3, J7:1)`specifies that `J7:3` is the signal connection for the `DVM` and `J7:1` is the ground sense connection for the `DVM`.

3. Potentiometer adjustment step. This step allows interactive adjustment of a potentiometer. CALDAP displays the letter of a particular potentiometer and a sequence of arrows which indicate the direction in which to turn the potentiometer. Turn the potentiometer until the arrow display is centered and the arrows are replaced by a vertical line.

During calibration, the following keys perform control functions:

```
<enter> goes to next step
<backspace> goes to previous step
<esc> aborts calibration
```

After aborting or finishing calibration, a `<Ctrl-Z>` command from the keyboard will end the CALDAP program. Optionally, the user may enter a `<Ctrl-E>` command from the keyboard to restart calibration. Several calibration sequences are iterative—a series of calibration steps is repeated until potentiometer adjustments are sufficiently accurate. In most cases no iteration is required during recalibration; if a particular potentiometer is adjusted more than three times, CALDAP probably has detected instability in the calibration sequence. This usually is caused by excessive noise in the adjustable external voltage supply, or possibly by damaged analog circuitry on the Data Acquisition Processor.

Calibrating Simultaneous Sampling Boards

CALDAP also can be used to calibrate the Microstar Laboratories Simultaneous Sampling Boards models MSXB 010-01 and MSXB 011-01. Calibration files for simultaneous sampling boards are stored in the subdirectories `\DAP\CALDAP\MSXB010` and `\DAP\CALDAP\MSXB011` on the Data Acquisition Processor diskettes. Contact Microstar Laboratories for additional calibration information.

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