DAP 4000a Manual

Installation Guide and
Connector Reference

Version 1.11

Microstar Laboratories, Inc.

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Part Number DAP4000AM111

Contents

1. Introduction

The Data Acquisition Processor from Microstar Laboratories is a complete data acquisition system that occupies one expansion slot in a PC. Data Acquisition Processors are suitable for a wide range of applications in laboratory and industrial data acquisition and control.

The DAP 4000a is a high-performance Data Acquisition Processor suitable for high-speed data acquisition and control.

Features of the DAP 4000a:
- TI486SXLC2-50 CPU
- PCI bus interface
- 14-bit A/D converter
- 50 ns TIME resolution
- 800K samples per second
- ±2.5 volt, ±5 volt, 0-5 volt, and ±10 volt analog input ranges
- ±2.5 volt, ±5 volt, 0-5 volt, 0-10 volt, and ±10 volt analog output ranges

The onboard operating system for the DAP 4000a is DAPL 2000, which is optimized for 32 bit operation.

About This Manual

This manual includes hardware and software installation instructions, a hardware connector reference, hardware operation reference, and recalibration instructions. Two other manuals provide information about creating data acquisition applications:
- The DAPL Manual contains a complete DAPL reference.
- The Applications Manual contains many useful examples of Data Acquisition Processor applications.

2. Installation, Testing, & Troubleshooting

Installing a Data Acquisition Processor involves the following steps:

1. Install the Data Acquisition Processor.
2. Install the DAP Software.
3. Test the Installation.

Installation instructions are provided in this chapter. If there are any problems with installation, please read the troubleshooting guide at the end of this chapter.

Data Acquisition Processor Handling Precautions

Static control is required for handling all electronic equipment. The Data Acquisition Processor is especially sensitive to static discharge because it contains many high-speed analog and digital components. To protect the Data Acquisition Processor, observe the following precautions:

- Wear a grounding strap when handling the Data Acquisition Processor. If it is not possible to use a grounding strap, continuously touching a metal screw on a grounded PC offers protection.
- If it is necessary to transport the Data Acquisition Processor outside of the PC, be sure to shield the Data Acquisition Processor in a conductive plastic bag. If a conductive bag is not available, shield the Data Acquisition Processor by wrapping it completely in aluminum foil. Do not ship or store a Data Acquisition Processor in plastic peanuts without suitable shielding.

Static damage to analog components can cause subtle problems, including oscillation, increased settling time, and reduced slew rate. If you suspect that a Data Acquisition Processor has been affected by static discharge, return it to Microstar Laboratories for testing, repair, and quality control.

System Requirements

The DAP 4000a is compatible with 5V 32 bit PCI Bus slots that support bus-mastering in 486/Pentium/Pentium Pro/Pentium II/Pentium III computers and requires Windows 95, Windows 98 or Windows NT 3.51 or later.

Installing the Data Acquisition Processor

Caution: Do not install the Data Acquisition Processor while the PC is on.

To Install the Data Acquisition Processor:

1. Turn off the PC and remove the PC's cover.
2. Insert the Data Acquisition Processor into any free PCI slot.
3. Screw down the back panel of the Data Acquisition Processor to the back chassis of the PC.

The Data Acquisition Processor requires approximately 15 Watts from the PC's power supply. If your system behaves erratically with the Data Acquisition Processor installed, the PC may need a larger power supply.

Installing Several Data Acquisition Processors

Many Data Acquisition Processor boards can operate simultaneously in one PC. Running several boards in parallel increases the maximum sampling rate and the real-time processing power of a system. The driver supports up to 14 Data Acquisition Processor boards in one PC. However, the number of Data Acquisition Processor boards is limited by the number of available PCI slots in the PC.

Installing DAP Software

When you insert the DAPtools CD into your CD-ROM drive, the Microstar Laboratories Setup Launcher will automatically run. When you select the 'Getting Started' link, you will obtain instructions for installing DAP software.

If the Windows hardware installer asks for the INF file, you can find the MSLACOM.INF file at the root of the DAPtools CD.

You can obtain more detailed instructions for installing DAP software under various operating systems by selecting the 'Documentation' link, followed by 'DAPtools Basic|Accel32|Installation'.

Testing Installation

To test the software installation, run the `DAPlog.EXE` program.

Troubleshooting

If the Accel32 Service will not start, check the host PC hardware manual to make sure that the particular PCI slot that the DAP uses supports bus-mastering. If necessary, switch to a different slot.

3. DAP 4000a Connectors

This chapter discusses the interface connectors on the DAP 4000a. Diagrams and documentation for the analog input/output connector, the digital input/output connector, the output clock connector, and jumpers are provided in this chapter. Also included are detailed instructions for setting the following options:

- the analog input voltage range (J7, J8, J9, & J14)
- the output voltage ranges of DAC0 and DAC1 (J11 and J12)
- the digital output polarity at power-on (J32)
- input/output synchronization (J22)

Figure 1 shows component placement outlines of the DAP 4000a. The only components shown are connectors, whose labels begin with the letter J, some integrated circuits, whose labels begin with the letter U, and trim potentiometers, whose labels are single letters.

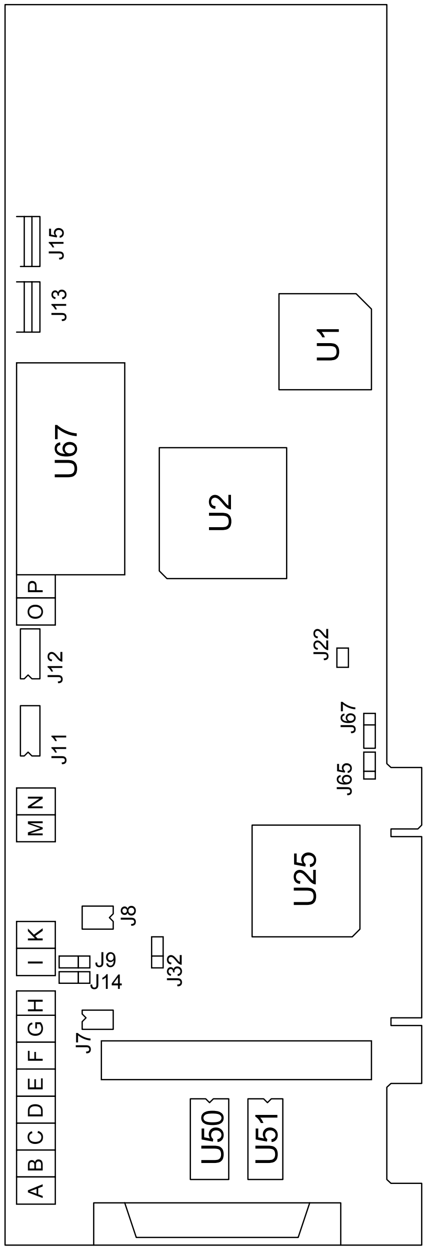


Figure 1.
DAP 4000a

Analog Input/Output Connector

Analog voltages are connected to the Data Acquisition Processor through a 68-pin connector on the back panel of the PC. This connector is located on the left side of the Data Acquisition Processor and is labeled `J2 ANALOG IN/OUT`. It has a double row of pins on 0.050 inch centers. The connector is 3M part number 10268-52E2VC or AMP part number 2-178238-8. It mates with discrete wire connector 3M part number 10168-6000EC or AMP 2-175677-8. Both connectors are shielded and are compatible with round cable. The analog I/O connector also mates with insulation displacement ribbon cable connector 3M part number 10168-8100EE. The insulation displacement connector is compatible with 0.025" pitch ribbon cable.

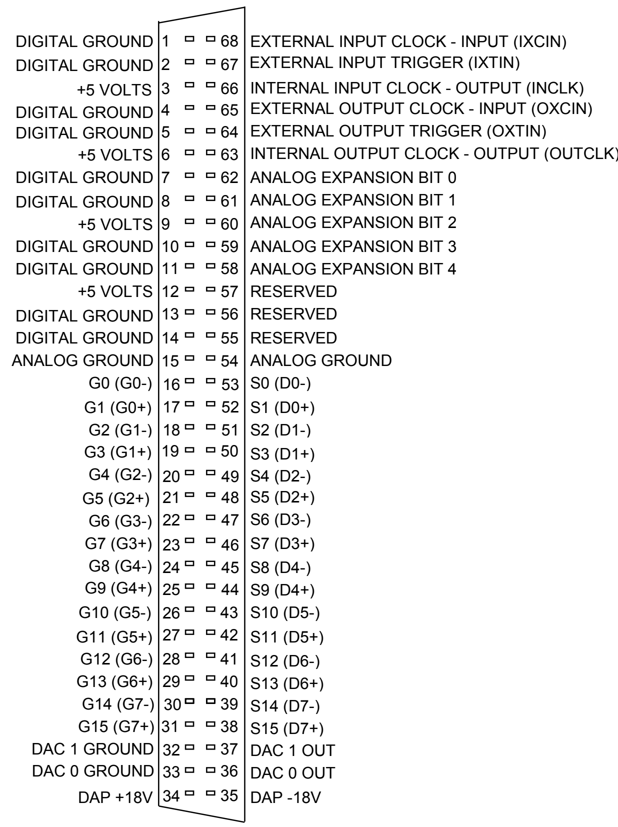
There are two base models of the DAP4000a. The pin numbering assignments for the two base models are the same except for pins 58 through 62. For the DAP4000a/112, these pins are reserved. For the DAP4000a/212, these pins are used for analog expansion.

Looking at the DAP 4000a/112 connector from the back of a PC, the pin numbering is:

DIGITAL GROUND	1	68	EXTERNAL INPUT CLOCK - INPUT (IXCIN)
DIGITAL GROUND	2	67	EXTERNAL INPUT TRIGGER (IXTIN)
+5 VOLTS	3	66	INTERNAL INPUT CLOCK - OUTPUT (INCLK)
DIGITAL GROUND	4	65	EXTERNAL OUTPUT CLOCK - INPUT (OXCIN)
DIGITAL GROUND	5	64	EXTERNAL OUTPUT TRIGGER (OXTIN)
+5 VOLTS	6	63	INTERNAL OUTPUT CLOCK - OUTPUT (OUTCLK)
DIGITAL GROUND	7	62	RESERVED
DIGITAL GROUND	8	61	RESERVED
+5 VOLTS	9	60	RESERVED
DIGITAL GROUND	10	59	RESERVED
DIGITAL GROUND	11	58	RESERVED
+5 VOLTS	12	57	RESERVED
DIGITAL GROUND	13	56	RESERVED
DIGITAL GROUND	14	55	RESERVED
ANALOG GROUND	15	54	ANALOG GROUND
G0 (G0-)	16	53	S0 (D0-)
G1 (G0+)	17	52	S1 (D0+)
G2 (G1-)	18	51	S2 (D1-)
G3 (G1+)	19	50	S3 (D1+)
G4 (G2-)	20	49	S4 (D2-)
G5 (G2+)	21	48	S5 (D2+)
G6 (G3-)	22	47	S6 (D3-)
G7 (G3+)	23	46	S7 (D3+)
G8 (G4-)	24	45	S8 (D4-)
G9 (G4+)	25	44	S9 (D4+)
G10 (G5-)	26	43	S10 (D5-)
G11 (G5+)	27	42	S11 (D5+)
G12 (G6-)	28	41	S12 (D6-)
G13 (G6+)	29	40	S13 (D6+)
G14 (G7-)	30	39	S14 (D7-)
G15 (G7+)	31	38	S15 (D7+)
DAC 1 GROUND	32	37	DAC 1 OUT
DAC 0 GROUND	33	36	DAC 0 OUT
DAP +18V	34	35	DAP -18V

Note: Use the pin numbering on this chart, rather than numbers which may be found on your connector. Connectors from different manufacturers are not numbered consistently.

Looking at the DAP4000a/212 connector from the back of a PC, the pin numbering is:



Note: Use the pin numbering on this chart, rather than numbers which may be found on your connector. Connectors from different manufacturers are not numbered consistently.

Single-ended inputs are indicated by `S0` through `S15`; their corresponding ground inputs are `G0` through `G15`. Differential inputs are indicated by `D0-` and `D0+` through `D7-` and `D7+`; their corresponding ground inputs are `G0-` and `G0+` through `G7-` and `G7+`. Every differential signal must be referenced to the corresponding ground. Data Acquisition Processors have a limited common mode voltage range, and a ground connection must be used to assure that this range is not exceeded.

A single-ended analog signal should be connected to an analog ground pin and to an analog input pin, for example to pins 16 and 53. A differential analog signal should be connected to two adjacent analog input pins and either of their corresponding grounds, for example to input pins 52, 53, and ground pin 16 or 17.

Termination boards to connect all lines of the analog connector to discrete wires are available from Microstar Laboratories.

The DAP 4000a features fault-protected input multiplexers. Fault protected input multiplexers allow signals to be connected to the Data Acquisition Processor with power off and allow a higher input voltage without damaging the inputs. Spare fault-protected input multiplexers are available from Microstar Laboratories.

Analog input signals should be within the range from -25 volts to +25 volts, relative to the ground of the Data Acquisition Processor. Input signals may be applied to the Data Acquisition Processor when the PC's power is off. See Chapter 5 for electrical characteristics of the analog input pins.

The analog I/O connector of the Data Acquisition Processor includes digital-to-analog converter output pins and analog supply voltages. Pins 36 and 37 are the outputs of `DAC0` and `DAC1`, respectively. Pins 33 and 32 are the grounds for `DAC0` and `DAC1`, respectively. The digital-to-analog converters have voltage outputs with typical output impedance of 0.05 Ohms. These normally should drive high impedance inputs. The output current from each digital-to-analog converter output is rated at ±5 milliamps, but it is recommended that this current not exceed ±1 milliamp.

Analog outputs are set to zero when the system is first powered on. When analog outputs are configured for unipolar mode, the outputs are set to half of the full scale range when the system is first powered on. When `J32` is moved, the analog outputs at power-on may vary by up to 5 millivolts.

Pin 15 is analog power ground. Pins 34 and 35 are connected to +18 volt and -18 volt analog supplies. The maximum allowable current drain from these supplies is 20 milliamps per side. These supplies can be used for low current, low noise devices such as external multiplexers. To supply power to other devices, either use an external supply or use the 5 volt digital power supply found on the analog control connector with an external DC-to-DC converter.

The analog I/O connector also provides an external trigger input, an external input clock input, an internal input clock output, and connections to the 5-volt digital supply and its ground.

In addition, the DAP4000a/212 provides analog input expansion control lines. Pins 58 through 62 of the analog I/O connector provide TTL-compatible analog input expansion control signals that select the expansion port. The five highest order bits of the input pin number appear in descending order on pins 58, 59, 60, 61, and 62 for a period starting one sample time before the analog input is sampled.

External analog input expansion boards are available from Microstar Laboratories. Each input expansion board allows up to 32 differential inputs, or up to 64 single-ended inputs, or any combination requiring up to 64 input lines. A DAP4000a/212 can control up to 8 external expansion boards, for a total of 512 input lines.

The analog I/O connector has an input pin for an active high external trigger. Sampling is inhibited if the external trigger is inactive when an input procedure is started. Sampling then commences on the inactive to active transition.

The external trigger is either one-shot or gated, depending on the `HTRIGGER` command in the active input procedure. The external trigger is ignored if there is no `HTRIGGER` command in the active input procedure. See Chapter 6 for more information.

An external trigger signal must be within the standard TTL logic range of 0 to +5 volts. The Data Acquisition Processor provides a pull-up resistor on the external trigger input. This forces the trigger input active if it is left unconnected.

Clock and trigger inputs may have signals applied when the Data Acquisition Processor is off.

The analog I/O connector has input and output pins for an external input clock. The input pin should be used to connect an external input clock. The output pin is the buffered output of the internal clock circuit. See Chapter 6 for more information.

Pins 3, 6, 9, and 12 provide +5 volt power. Maximum current from the +5 volt supply is 1 Amp.

Digital Input/Output Connector

The digital input/output connector is a vertical 100-pin connector labeled `J1`. This connector is near the left edge of the Data Acquisition Processor, to the right of the analog input/output connector. The digital I/O connector has two rows of 50 pins on 0.050 inch centers. This connector is manufactured by AMP, part number 1-104549-0. The digital I/O connector mates with insulation displacement connector AMP 1-111196-6.

The digital I/O connector is not accessible from the back of the PC. A cable, part number MSCBL 042, that makes the digital connector accessible at the adjacent slot in the PC is available from Microstar Laboratories. For systems that comply with the European EMC Directive, MSCBL 076 provides the same functionality as MSCBL 042, but with a shielded connector. Contact Microstar Laboratories for more information.

The pin numbering of the digital input/output connector is shown in the following diagram:

Signal	Pin	Pin	Signal
RESERVED	51	50	RESERVED
DIGITAL GROUND	52	49	+5 VOLTS
DOUT 15	53	48	DIGITAL GROUND
DOUT 14	54	47	DIGITAL GROUND
DOUT 13	55	46	DIGITAL GROUND
DOUT 12	56	45	+5 VOLTS
DOUT 11	57	44	DIGITAL GROUND
DOUT 10	58	43	DIGITAL GROUND
DOUT 9	59	42	DIGITAL GROUND
DOUT 8	60	41	+5 VOLTS
DOUT 7	61	40	DIGITAL GROUND
DOUT 6	62	39	DIGITAL GROUND
DOUT 5	63	38	DIGITAL GROUND
DOUT 4	64	37	+5 VOLTS
DOUT 3	65	36	DIGITAL GROUND
DOUT 2	66	35	DIGITAL GROUND
DOUT 1	67	34	DIGITAL GROUND
DOUT 0	68	33	+5 VOLTS
INTERNAL OUTPUT CLK - OUTPUT	69	32	DIGITAL GROUND
RESERVED	70	31	DIGITAL GROUND
RESERVED	71	30	DIGITAL GROUND
RESERVED	72	29	+5 VOLTS
RESERVED	73	28	DIGITAL GROUND
RESERVED	74	27	DIGITAL GROUND
RESERVED	75	26	DIGITAL GROUND
RESERVED	76	25	+5 VOLTS
RESERVED	77	24	DIGITAL GROUND
RESERVED	78	23	DIGITAL GROUND
RESERVED	79	22	DIGITAL GROUND
DX2	80	21	+5 VOLTS
DX1	81	20	DIGITAL GROUND
DX0	82	19	DIGITAL GROUND
INTERNAL INPUT CLK - OUTPUT	83	18	DIGITAL GROUND
DIN 15	84	17	+5 VOLTS
DIN 14	85	16	DIGITAL GROUND
DIN 13	86	15	DIGITAL GROUND
DIN 12	87	14	DIGITAL GROUND
DIN 11	88	13	+5 VOLTS
DIN 10	89	12	DIGITAL GROUND
DIN 9	90	11	DIGITAL GROUND
DIN 8	91	10	DIGITAL GROUND
DIN 7	92	9	+5 VOLTS
DIN 6	93	8	DIGITAL GROUND
DIN 5	94	7	DIGITAL GROUND
DIN 4	95	6	DIGITAL GROUND
DIN 3	96	5	+5 VOLTS
DIN 2	97	4	DIGITAL GROUND
DIN 1	98	3	DIGITAL GROUND
DIN 0	99	2	DIGITAL GROUND
+5 VOLTS	100	1	DIGITAL GROUND

Pins 1 and 100 are closest to the gold edge fingers.

Digital inputs are indicated by `DIN 0-15` and digital outputs are indicated by `DOUT 0-15`. Bit 0 is the least significant bit.

A termination board from Microstar Laboratories, part number MSTB 008, connects all lines of the digital connector to discrete wire connectors.

The digital inputs are FCT TTL with 10K pull-up resistors. The digital inputs sink no more than 5 microamps for a “1” input and source no more than 0.5 milliamps for a “0” input. An input voltage greater than 2V is interpreted as a “1” and an input voltage less than 0.8V is interpreted as a “0”. When no signal is connected, a digital input is read as a “1” due to the pull-up resistors.

Digital inputs may have TTL signals applied when the Data Acquisition Processor is off.

Digital output polarity at power-on is selected by `J32`, the Digital Output Reset Polarity Jumper, described later in this chapter.

The digital outputs are FCT TTL; they can sink no more than 12 milliamps for a “0” output and can source no more than 15 milliamps for a “1” output. The output voltage for a “1” is greater than 2.4 V and the output voltage for a “0” is less than 0.50 V.

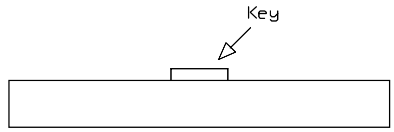
The digital input/output connector has multiple connections to the Data Acquisition Processor +5 V power supply. The supply current is rated at 500 milliamps per connection with a total current limit of 2 Amps. The 2 Amp current limit is due to the limited current available from the host computer.

Pins 80, 81, and 82 provide TTL-compatible digital input expansion control signals. The low-order bit of the port number appears on pin 82, the middle bit appears on pin 81, and the high-order bit appears on pin 80.

An optional digital input port may be specified in a DAPL `SET` command. The digital input port numbers range from 0 to 7. The specified port number appears on the control pins for a period starting one sample time before the time at which the digital inputs are sampled. The port number can be used to control external multiplexers.

An external digital expansion board is available from Microstar Laboratories. Each external expansion board allows up to 64 digital inputs and 64 digital outputs.

The Microstar Laboratories cable MSCBL 036 01 is compatible with the digital input/output connector. The diagram below shows the key on the cable. This key must be towards the left side of the Data Acquisition Processor.



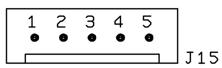
Note: Cables not made by Microstar Laboratories may have different keys.

Output Clock Connector

Connector `J15` is a five pin connector, Molex part number 22 23 2051; the mating connector is Molex part number 22 01 3057. `J15` is located on the top edge of the Data Acquisition Processor, near the right side of the board.

The output clock signals and the output trigger signal are on connector `J15`, along with power and ground. These signal pins can be used to control when outputs are updated. See Chapter 6 for more details.

The pin numbering for `J15` is given in the following table:




```
Pin 1  Ground
Pin 2  External output trigger - input
Pin 3  Internal output clock - output
Pin 4  External output clock - input
Pin 5  +5 volts
```

Shunts

Several of the Data Acquisition Processor options are set by shunts. These are jumper wires enclosed in plastic, designed for connecting pins on 0.100" centers.

Each shunt has a top and a bottom. When a shunt is placed correctly, a probe point is visible in the shunt. Shunts must not be placed upside down on the pins, as incorrectly placed shunts do not provide reliable contacts.

Analog Signal Path Selection

In addition to the DAPL configuration options, the Data Acquisition Processor has several hardware configuration options. These determine the path taken by analog signals from the input pins to the analog-to-digital converter.

The analog signal path between the input pins and the analog-to-digital converter consists of the following functional units:

1. input multiplexers

2. instrumentation amplifier
3. programmable gain amplifier
4. range amplifier
5. analog-to-digital converter with sample-and-hold amplifier

Analog signals must pass through the input multiplexers, the instrumentation amplifier, and the analog-to-digital converter. Jumpers determine whether the analog signal path includes the programmable gain amplifier and the range amplifier, and also determine the input voltage range.

A signal range is called bipolar if it includes both positive and negative voltages; a signal range is called unipolar if it includes voltages of only one sign. The range amplifier allows the bipolar analog-to-digital converter to operate with unipolar voltages. Jumpers select from three bipolar ranges and one unipolar range. If the programmable gain amplifier is enabled, gains of 1, 10, 100, and 500 are software selectable.

Analog Signal Path Configuration

Four connectors control the analog signal path of the DAP 4000a. Note that changing voltage ranges may require recalibration.

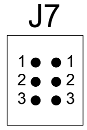
The following table summarizes the DAP 4000a analog input jumper connections:

ADC Range	**J7**	**J8**	**J9**	**J14**
0 to 5 v	2	3	1 - 2	1 - 2
± 2.5v	1	2	2 - 3	1 - 2
± 5v*	2 *	3 *	2 - 3 *	1 - 2 *
± 10 v	2	3	2 - 3	2 - 3

* Factory Configuration

The input signal to the range amplifier is selected by `J7`.

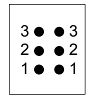
J7



Exactly one jumper should be placed on `J7`, as follows:

Jumper	**Range amplifier input**
1	range amplifier disabled
2	programmable gain amplifier
3	instrumentation amplifier

The input signal to the analog-to-digital converter is selected by `J8`.



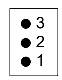
J8

Exactly one jumper should be placed on `J8`, as follows:

Jumper	**Analog-to-digital converter input**
1	instrumentation amplifier
2	programmable gain amplifier
3	range amplifier

Note that jumpers on `J7` and `J8` are placed horizontally.

The signal range of the range amplifier is selected by `J9` and `J14`. `J9` selects between unipolar inputs and bipolar inputs.

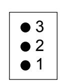


J9

One jumper should be placed on `J9` as follows:

Jumper	**Signal range**
1-2	unipolar
2-3	bipolar

`J14` selects the input signal range of the range amplifier.



J14

One jumper should be placed on `J14` as follows:

Jumper	**Input signal range**
1-2	0 to 5 Volts
1-2	± 2.5 Volts
1-2	± 5 Volts
2-3	± 10 Volts

Note: Regardless of the input voltage range, positive and negative differential signals may range from -25 volts to +25 volts without damaging the Data Acquisition Processor .

Note: There is a maximum speed reduction for the ±10-volt input range in order to get 14-bit accuracy on the DAP 4000a. Using the input voltage range of ±10 volts, the minimum `TIME` is 2.4 µs, which is approximately 417K samples/second.

Analog Output Voltage Range Selection

The voltage ranges of DAC0 and DAC1 are selected by headers J11 and J12, respectively:

J11 J12

Three or four jumpers should be placed on J11 and J12, as follows:

Jumpers	**Range**
2-3, 8-9, 4-5, 6-7	0 to 5 Volts
2-3, 8-9, 6-7	0 to 10 Volts
1-2, 9-10, 4-5, 6-7	± 2.5 Volts
1-2, 9-10, 6-7	± 5 Volts
1-2, 9-10, 5-6	± 10 Volts

Note: By default, DAPL assumes that the outputs of the digital-to-analog converters are bipolar. If a unipolar output range is selected, the following DAPL command must be issued: `OPTION BPOUTPUT=OFF`

Digital Output Reset Polarity Jumper

The digital output reset polarity jumper J32 has three pins spaced at 0.100". J32 is located in the upper left section of the Data Acquisition Processor , directly to the right of J1.

The digital output reset polarity jumper allows selection of the digital output polarity at power-on. If the shunt is installed on pins 1-2 (pin 1 is on the left) of J32, all digital outputs will be reset to 0 at power-on. If the shunt is installed on pins 2-3 of J32, all digital outputs will be preset to 1 at power-on. All Data Acquisition Processors are shipped from the factory with shunts installed on pins 1-2 of J32. The voltage of the analog outputs at reset may vary by up to 5 millivolts when the shunt on J32 is moved.

Input/Output Synchronization Header

The input/output synchronization header J22 has two pins spaced at 0.100". J22 is located approximately one inch to the right of the right set of gold fingers on the Data

Acquisition Processor. If a shunt is placed on `J22`, the input trigger is connected to the output update clock. This causes a hardware input trigger to occur when an output procedure initiates its first update. This is used to synchronize input sampling to output updates.

Synchronization Connector

The synchronization connector `J13` has a single row of five pins on 0.100 inch centers. `J13` is located along the top edge of the Data Acquisition Processor near the right side of the board. The synchronization connector allows several Data Acquisition Processors to share the same sampling clock.

For synchronization, the shared sampling clock requires special cabling between Data Acquisition Processors. The analog sampling clock of the master unit is supplied to the slave units by means of the cable MSCBL 015-01. Contact Microstar Laboratories for more information about cabling for synchronous Data Acquisition Processors.

Note: When synchronizing the DAP 4000a with ISA bus models of Data Acquisition Processors, the DAP 4000a must be configured as the slave unit. When synchronizing the DAP 4000a with PCI bus models of Data Acquisition Processors, the DAP 4000a can be configured as either master or slave.

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4. Analog Input Circuits

The analog input hardware of the Data Acquisition Processor is discussed in some detail in this chapter. The following summary gives sufficient information for most Data Acquisition Processor applications:

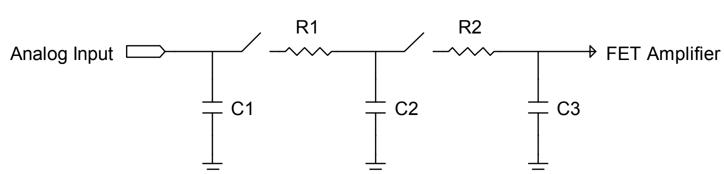
- The DC input impedance is very high.
- At high sampling rates, the signal source impedance should be low.
- Minimum sampling times are specified for unity gain.
- At gain 10, the fastest sampling rate is slower than the fastest sampling rate at gain 1.
- At gain 100 and 500, the fastest sampling rate is substantially slower than the fastest sampling rate at gain 1.

Analog Input Circuits

Data Acquisition Processor analog input signals pass through two analog multiplexers and then to an op amp with a FET input. The DC input impedance is very high, typically far in excess of 10M Ohms. The AC input impedance is dominated by the capacitance of the multiplexers.

Figure 2 shows a useful equivalent circuit for each Data Acquisition Processor input. As the Data Acquisition Processor scans through the input pins defined by an input procedure, the switches in the multiplexers open and close, connecting the specified inputs to multiplexer outputs. When an input signal is connected to the FET amplifier, the signal source must supply sufficient current to charge the equivalent capacitance of the multiplexers before the analog-to-digital conversion can start.

Figure 2



The DAP 4000a has fault-protected multiplexers. The following table shows typical resistance and capacitance values, in Ohms and picofarads, for fault-protected multiplexers.

Component	**Value**
R1	300Ω
R2	100Ω
C1	5 pF
C2	55 pF
C3	30 pF

Programmable Gain Amplifier

At gains other than unity, the programmable gain amplifier requires extra time to switch from one channel to another and then settle to full accuracy. The following table shows typical minimum sampling times for the DAP 4000a at each gain.

Minimum Sample Times in μS at Gain:

	1	**10**	**100**	**500**
DAP 4000a	1.25	8	40	500

5. Clocks and Triggers

The Data Acquisition Processor is designed to operate using either internal clocks or external clocks. The Data Acquisition Processor has onboard crystal-controlled timers to provide an internal input sampling rate and output update rate, and also has provisions for external clocks for both input and output.

The Data Acquisition Processor has hardware control lines for an input clock, an output clock, an input trigger, and an output trigger. These lines all are TTL compatible. The input clock and the output clock both are positive-edge triggered.

The input and output clocks of the DAP 4000a have two modes. In the first mode, called Channel List Clocking, the Data Acquisition Processor starts conversion of an entire channel list on the positive edge of the clock. In the second mode, the Data Acquisition Processor converts a single channel on the positive edge of the clock.

The input trigger and output trigger on all models also have two modes, a one-shot mode and a level-triggered gate mode.

Software Triggers vs. Hardware Triggers for Input

DAPL provides a powerful software triggering mechanism which is suitable for most applications. For those applications which require precise synchronization to external hardware or which are too fast to take advantage of software triggering, hardware triggering is provided. Software triggering is more versatile than hardware triggering. Except in applications with high sampling rates combined with demanding processing requirements, software triggering almost always provides a better solution than hardware triggering.

Software triggers rely on DAPL tasks to scan input data to detect events within the data. When an event is detected, a task asserts a software trigger. After the trigger is asserted, another task may act, based on the assertion. The most common action is to pass a number of values around the trigger event either to another task or to the PC. The trigger mechanism is much like the trigger on an oscilloscope. Since all of the processing functions of DAPL may be used to define events, however, much more complex events may be detected.

Hardware input triggers are implemented using a digital control line which is separate from the sampling stream. This control line starts and stops input sampling. Since the trigger line is not dependent on the input data, external hardware must be provided to detect events of interest.

Software triggers have several advantages over hardware triggers. First, a software trigger may be changed by changing a few lines in a DAPL command list. In contrast, a hardware trigger event must be detected by external hardware which may be inflexible and costly to modify. Second, software triggers scan input data to detect events, so pretrigger data are available. Because a hardware trigger starts the Data Acquisition Processor input section, no samples are taken before a trigger event. Finally, with software triggers, DAPL provides precise timing information. With hardware triggers, DAPL is not able to provide accurate timing information because hardware triggers start and stop input sampling at undefined times.

Hardware triggering does provide precise synchronization of acquisition to external events. Hardware triggering also allows detection of events which are too fast to process with software triggers.

Software and hardware triggers are implemented separately and may be used together.

External Input Clock

For most applications, there is no need to provide an input clock source to the Data Acquisition Processor; the on-board timer provides a wide range of sampling frequencies with fine time resolution. The main use of an external input clock is to precisely match the sampling rate to a standard frequency.

The external input clock is a positive-edge triggered TTL signal. The external input clock is activated by the command `CLOCK EXTERNAL` in an input procedure. The `TIME` command of an input procedure with input clocking enabled must be at least tSYNCH less than the period of the external clock. tSYNCH is defined at the end of this chapter.

External input clocking has two modes. The first mode, called Channel List Clocking, starts conversion of an entire channel list on the positive edge of the external clock. The second mode converts a single channel on the positive edge of the external clock. The selection between the modes is made by a parameter to the `CLCLOCKING` command in an input procedure. The two options for `CLCLOCKING` are `ON` and `OFF`. The default is `ON`.

Example:

```
IDEF A 5
   CLOCK EXTERNAL
   CLCLOCKING ON
   SET IP0 S0
   SET IP1 S1
   SET IP2 S2
   SET IP3 S3
   SET IP4 S4
   TIME 1000
   . . . .
   END
```

External input clocking is enabled for the input procedure `A`. With Channel List Clocking selected, each positive edge of the external clock causes conversion of the entire channel list consisting of channel 0 (`S0`) to channel 4 (`S4`). The channels are converted in sequence with channel 0 synchronized to the positive edge of the external clock and each of the subsequent channels converted according to the `TIME` command. Channel 1 (`S1`) is converted 1000 µs following the edge of the external clock, channel 2 (`S2`) is converted 2000 µs following the edge of the external clock, up to channel 4 (`S4`) which is converted 4000 µs following the edge of the external clock. When using Channel List Clocking, the period of the external clock (rising edge to rising edge) must be greater than the `TIME` command times the number of channels plus tSYNCH. The external clock may be as slow as required—there is no maximum period.

If single channel clocking is selected rather than Channel List Clocking, each positive edge of the external clock causes conversion of only one channel. The channels are converted in sequence. Each channel is synchronized to a positive edge of the external clock. In the previous application, channel 0 (`S0`) is converted on the first edge of the external clock, channel 1 (`S1`) is converted on the second edge of the external clock, and so on up to channel 4 (`S4`), which is converted on the fifth edge of the external clock. The channel list then is repeated with channel 0 converted again on the sixth positive edge of the external clock. When using single channel clocking, the period of the external clock (rising edge to rising edge) must be greater than the `TIME` command plus tSYNCH. The external clock may be as slow as required; there is no maximum period.

Input Pipeline

The DAP 4000a has one pipeline stage for analog and digital inputs. An input is acquired and read by the CPU on the same input clock cycle. Note that this is an improvement over the DAP 3200a pipeline, where an input is acquired on one input clock cycle, and that acquired value is read by the CPU on the next input clock cycle.

The DAP 3200a and other ISA bus models of Data Acquisition Processors generate an additional input clock cycle when input sampling is stopped, in order for the CPU to read the last acquired value. When synchronizing multiple Data Acquisition Processors, the master generates the additional input clock cycle. The slave units depend on this additional clock cycle to read the last acquired value.

Because of its improved input pipeline, the DAP 4000a does not generate an additional input clock when input sampling is stopped. Therefore, the DAP 4000a must be configured as a slave unit when synchronizing the DAP 4000a with other ISA bus models of Data Acquisition Processors.

The other PCI bus models of Data Acquisition Processors share the same single pipeline stage as the DAP 4000a. Therefore, the DAP 4000a can be configured as either master or slave when synchronizing it with other PCI bus models of Data Acquisition Processors.

It is important to note that if the first channel in an input configuration is a counter/timer input, there will be one more clock period delay added to the pipeline. This additional delay is usually not desirable; therefore, it is strongly recommended that the first channel of an input configuration be of any type other than counter/timer if possible. Also, the minimum sample time is 3.0 µs when the counter/timer board is used.

External Output Clock

For most applications, there is no need to provide an output clock source to the Data Acquisition Processor; the on-board timer provides a wide range of update frequencies with fine time resolution. The main use of an external output clock is to precisely match the output update rate to a standard frequency.

The external output clock on the Data Acquisition Processor is a positive-edge triggered TTL signal. Similar to the external input clock, the output clock is activated by the command `CLOCK EXTERNAL` in an output procedure. The `TIME` command of an output procedure with output clocking enabled must be at least tSYNCH shorter than the external clock period. tSYNCH and other times are defined at the end of this chapter. Unlike the external input clock, the first external output clock pulse is recognized.

On the DAP 4000a, external output clocking has two modes. The first mode, called Channel List Clocking, starts output of an entire channel list on the positive edge of the external clock. The second mode outputs a single channel on the positive edge of the external clock. The selection between the modes is made by a parameter to the `CLCLOCKING` command in an output procedure. The two options for `CLCLOCKING` are `ON` and `OFF`. The default is `ON`.

Hardware Input Trigger

There are two modes for the input trigger. The first is a one-shot mode and the second is a level-controlled gated mode. The mode of the hardware trigger is selected by a parameter to the `HTRIGGER` command in an input procedure. The three options for `HTRIGGER` are `ONESHOT`, `GATED`, and `OFF`. The default is `OFF`.

In the one-shot mode, the trigger line is held in a low state when an input procedure is started. Input sampling does not start until the trigger line is high. Sampling continues until a `STOP` command is issued or the number of samples specified by the `COUNT` command of the input procedure is reached. The first sampled value is precisely synchronized to the trigger edge and all subsequent values are within ±tSYNCH of the `TIME` command of the input procedure. tSYNCH and other times are defined at the end of this chapter. The active period of the external input trigger must be greater than tTRIG_MIN to guarantee proper operation.

In the level-triggered gated mode, input sampling may start and stop repeatedly, depending on the level of the trigger signal. The input is sampled continuously when the trigger signal is high. Input sampling stops when the trigger signal is low. The active period of the output trigger must be less than tTRIG_MAX to guarantee that only one update occurs.

When input clocking is configured in Channel List Clocking mode, the input is stopped only at channel list boundaries. When input clocking is configured to clock single channels, the input is stopped on channel boundaries. The effect of this is that the start of sampling is precisely synchronized to the positive edge of the trigger signal, assuming that sampling has stopped. Sampling stops when the Data Acquisition Processor has completed sampling of either a channel list or a channel. When input sampling has been stopped with the gated trigger, synchronization of sampling to the positive edge of the trigger signal is the same as for the one-shot mode.

Hardware Output Trigger

There are two modes for the output trigger of Data Acquisition Processors. The first mode is a one-shot mode and the second mode is a level-controlled gated mode. The mode of the hardware trigger is selected by a parameter to the `HTRIGGER` command in an output procedure. The three options for `HTRIGGER` are `ONESHOT`, `GATED`, and `OFF`. The default is `OFF`.

In the one-shot mode, the trigger line is held in a low state when an output procedure is started. Output updating does not start until the trigger line is high. Updating continues until a `STOP` command is issued or the number of updates specified by the `COUNT` command of the output procedure is reached. The first updated value is precisely synchronized to the trigger edge and all subsequent values are within ±tSYNCH of the `TIME` command of the output procedure. tSYNCH and other times are defined at the end of this chapter. The active period of the external input trigger must be greater than tTRIG_MIN to guarantee proper operation.

In the level-triggered gated mode, output updating may start and stop repeatedly, depending on the level of the trigger signal. The output is updated continuously when the trigger signal is high. Output updating stops when the trigger signal is low. The active period of the output trigger must be less than tTRIG_MAX to guarantee that only one update occurs.

When output clocking is configured in Channel List Clocking mode, the output is stopped only at channel list boundaries. When output clocking is configured to clock single channels, the output may stop after any channel. The effect of this is that the start of output is precisely synchronized to the positive edge of the trigger signal, assuming that output has stopped. Output stops when the Data Acquisition Processor has completed output of either a channel list or a channel. When output has been stopped with the gated trigger, synchronization of output to the positive edge of the trigger signal is the same as for the one-shot mode.

Timing Considerations

When an external clock is used, the time of an event with respect to the start of sampling may only be determined if the period of the external clock is known. DAPL establishes event times as sample times. If the external clock period is variable or the period is unknown, the time of an event cannot be determined. The event's sample number may still be useful in other contexts. Note that the results of all frequency domain processing such as `FREQUENCY`, `FFT`, and `FIRFILTER` depend on the period of the external clock and may not be defined if the external clock period varies.

When hardware triggering is used, DAPL provides timing information relative to the start of each external trigger. In a case of a one-shot trigger, sampling or output updating starts on a single event so all timing information is relative to the trigger event. In the case of a gated trigger, sampling or output updating may start or stop at arbitrary times. Timing information may still be obtained if means are provided to distinguish one external trigger event from the next.

Using the Input Trigger with External Input Clocking

Input triggering may be used with external input clocking. When these functions are used together, however, precise synchronization of acquisition to a trigger edge is not available. The reason for the loss of synchronization is that the Data Acquisition Processor has no control over the external clock.

The Data Acquisition Processor acts upon the first external clock cycle after the trigger has been asserted, assuming input sampling has stopped. To guarantee recognition of an external trigger, the external trigger must occur at least tTCSETUP before the positive edge of the external clock.

Using the Output Trigger with External Output Clocking

Output triggering may be used with external output clocking. To guarantee recognition of an external clock, the external trigger must occur at least tTCSETUP before the positive edge of the external clock.

Timing tables

tSYNCH	200 ns	Time needed to synchronize an internal clock to an external clock
tTRIG_MIN	60 ns	Minimum high period for the input and output trigger
tEXTCLK_PW	25 ns	Minimum high or low period of an external clock
tTCSETUP	50 ns	External trigger to external clock setup time
tTRIG_MAX	250 ns	Maximum high period of the input trigger to guarantee a single conversion
tINSKEW	200 ns	Time from input clock or trigger to conversion value held
tOUTSKEW	30 ns	Time from output clock until start of DAC slewing

6. Recalibration

Each Data Acquisition Processor is burned in and then calibrated by Microstar Laboratories. The accuracy of this calibration is sufficient for most applications. Accuracy is affected by three factors:

- the operating temperature of the Data Acquisition Processor
- drift in the Data Acquisition Processor circuitry
- analog voltage range selection.

The operating temperature is determined by a number of factors. If the Data Acquisition Processor is operated inside a personal computer, the operating temperature is affected by the number of expansion boards, power supply rating, fan efficiency, etc.

Component drift depends on total operating time of the unit as well as the number of times the unit has been powered up and down.

Changes to analog voltage ranges may require that the Data Acquisition Processor be recalibrated.

For applications requiring high accuracy, occasional recalibration may be necessary. For high absolute accuracy, the Microstar Laboratories calibration sequence requires that measurements be made using a 4.5 digit digital voltmeter with a DC accuracy of .024% (244 ppm) or better. In most applications, only relative accuracy is important, so recalibration with a less accurate digital voltmeter may be acceptable. Calibration also requires a variable voltage source with high stability.

Because calibration requires significant setup time, it generally is best to send Data Acquisition Processors to Microstar Laboratories for recalibration. Calibration is available from Microstar Laboratories for a nominal fee.

7. Appendix A: Declaration of Conformity

Declaration of Conformity

Microstar Laboratories
2265 116th Avenue NE
Bellevue, WA 98004

Microstar Laboratories declares that the DAP 4000a conforms to the following Directive and Standards:

Electromagnetic Compatibility (EMC):

EMC Directive 89/336/EEC

EN 55022	Emission Standard
EN 50082-1	Immunity Standard

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